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RESEARCH AND DEVELOPMENT OF INSTRUMENTATION PROGRAM, VEHICLE PE--ETC(U)
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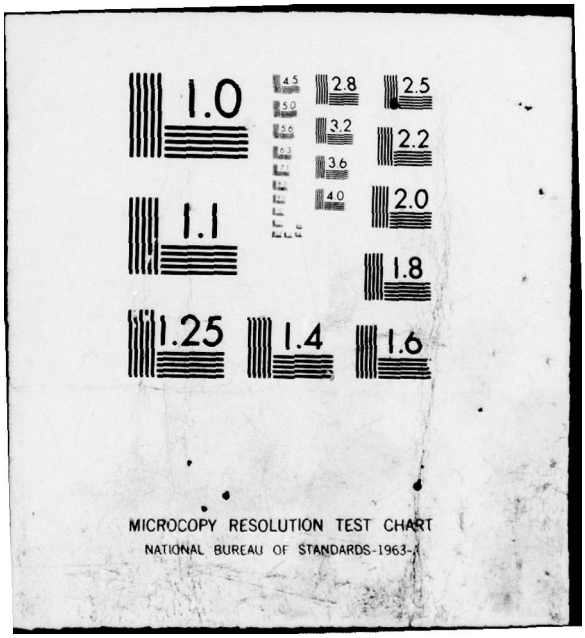
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FINAL REPORT

RESEARCH AND DEVELOPMENT

OF

INSTRUMENTATION PROGRAM, VEHICLE PERFORMANCE RECORDER

JUNE 1979

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US ARMY ABERDEEN PROVING GROUND
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At the present time automotive test data relative to use and operational environment is gathered by tachographs, analog tape recorders, and pulse code modulation (PCM) encoders. This project was to develop a Vehicle Performance Recorder (VPR) to augment the existing automotive test capability. The design objectives of the VPR were: self-contained, analog and digital inputs, digital recording, programmable, not require an on site or skilled operator, 8-hour capacity, 0.1% analog accuracy, 30-second time resolution, useable

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ABSTRACT

At the present time automotive test data relative to use and operational environment is gathered by tachographs, analog tape recorders, and pulse code modulation (PCM) encoders. This project was to develop a Vehicle Performance Recorder (VPR) to augment the existing automotive test capability. The design objectives of the VPR were: self-contained, analog and digital inputs, digital recording, programmable, not require an on site or skilled operator, 8-hour capacity, 0.1% analog accuracy, 30-second time resolution, useable in US Army Aberdeen Proving Ground (APG) environment, 28 VDC operation, and internal battery operation. A unit which meets these objectives is described in detail. The VPR uses a commercial cassette recorder and a custom controller to provide a flexible, low-power consumption data acquisition system. A description of alternative systems is also provided. It is concluded that: a) commercially manufactured units now exist with a wide spectrum of capabilities; c) the Army developed Vehicle Monitoring System (VMS) may be available in the future; d) no single unit satisifies all possible data acquistion requirements. It is recommended that a commercially available unit be used if possible; if not then the VPR be used.

FOREWORD

The Materiel Testing Directorate, US Army Aberdeen Proving Ground, was responsible for program planning, system development, fabrication, testing, and reporting. 2LT V. M. Lopez was responsible for input transducer and signal conditioning development, software development, and field testing.

SECTION 1. BODY

1. BACKGROUND

At the present time no single piece of instrumentation exists to gather use and operation environmental data during automotive testing. This type of data is important in determining that the same level of testing is applied to all vehicles and if properly analyzed should aid in predicting and evaluating failures. The type of indicators which are measured to provide this kind of information are listed in table 1-1. Additional applications include human factors engineering and vehicle course signature.

TABLE 1-1. USEAGE AND ENVIRONMENTAL INDICATORS

Oil temperature	Clutch operations
Oil pressure	Brake applications
Cooling system temperature	Time spent in each gear
Ambient temperature	Average speed
Electrical load	Average acceleration
Average rpm	Peak acceleration
Shock/vibration	

Tachographs are presently used to gather data on some of the indicators. However, the tachographs are not completely satisfactory since they are low resolution devices which must be analyzed by hand. At the other end of spectrum analog tape recorders and pulse code modulation (PCM) encoders are used when high-frequency, high-resolution, multichannel data acquisition is required. These instruments are very expensive, require an operator in attendance, and the analog recorder tape must be digitized before analysis can take place.

In order to bridge the gap between these extremes and augment the automotive test capability, a program to develop a vehicle performance recorder (VPR) was initiated.

2. OBJECTIVES

The objective of this program was to develop a data acquisition system for automotive testing which had the following characteristics:

a. Self-contained in a single enclosure which can be moved and installed by a single individual.

b. Able to accept both analog and digital transducer inputs.

c. Record the data in a digital format so that processing will be expedited.

d. Be programmable in terms of number of channels, type of channels (analog or digital), sequence of channels, and data rate.

e. Capable of unattended operation.

f. Not require a skilled operator.

g. Able to accept data for 8 hours without intervention.

h. 0.1% analog accuracy (acquisition system, not transducers).

i. Capable of 30-second time resolution.

j. Capable of operation in the standard test environment.

k. Able to operate from standard vehicle power (28 VDC) or from internal battery for up to 8 hours.

3. DETAILS OF PROJECT

3.1 RECORDING SYSTEM DESIGN

3.1.1 Selection of a Storage Medium

The two practical storage mediums available when the design began were solid-state memory and magnetic tape. Magnetic tape was chosen because it offered more storage per unit volume and more storage per unit power consumed than the solid state memory. In addition, the tape can be removed easily for the data analysis whereas the solid state memory cannot (a separate field retrieval capability would have to be supplied). The disadvantages of the magnetic tape are the maintenance of the recording mechanism, the cost of the tape itself, and the possiblility of data dropout.

3.1.2 Selection of a Recorder

Once the decision was made to use magnetic tape, an evaluation of commercial recorders was made. The criteria considered were:

a. Size.

b. Power consumption.

c. Ease of interface.

d. Ease of operation.

3.1.2 (Cont'd)

e. Ability to operate for 8 hours without intervention.

f. Environmental specifications.

The final choice was a Datel model LPS-16 write-only incremental digital cassette recorder using complimentary metal-oxide semiconductor (CMOS) electronics. The LPS-16 contains a 16-channel analog multiplexer and 12-bit analog to digital (A/D) converter for analog processing plus a separate input port for digital information. Some of the manufacturers specifications are:

a. Size: 4 by 4-1/2 by 7-1/2 inches (10.2 by 11.4 by 19.0 cm).

b. Power: 12 VDC; 80 milliamperes when recording, 10 microamperes during standby.

c. Temperature range: -10° to 60° C (14° to 140° F).

d. Relative humidity: 10% to 95% without condensation.

e. Weight: 2 pounds (9.1 kilograms).

f. Storage capacity: 120,000 16-bit words.

g. Data recording rate: five 16-bit words per second maximum.

Complete specifications and operating procedures are in reference 1.

The use of a standard tape cassette makes loading and operation easy. The use of external CMOS control circuitry makes the interface to the recorder straightforward. At a recording rate of four words per second, unattended recording for 8 hours is possible. The use of CMOS electronics and incremental recording keeps power consumption low so that battery operation is possible. A picture of the LPS-16 is in figure 3.1-1.

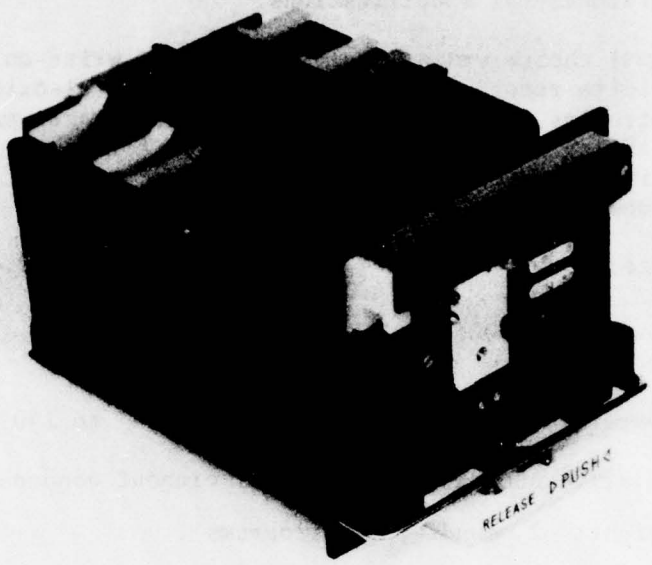


Figure 3.1-1. Cassette recorder used in VPR.

3.1.3 Controller Design

The recorder contains all of the electronics for A/D conversion and writing on tape. However, an external controller is required to provide system timing, sample rate selection, and number, sequence, and type of channel selection. The primary considerations in the controller design were:

a. Use of CMOS electronics, where possible, to ensure interface compatibility with the recorder.

b. Keep power consumption as low as possible.

c. Keep size as small as possible.

d. Provide as much flexibility in control as possible.

The important features of the controller design which evolved are:

a. A crystal controlled oscillator with dividers to provide a precise clock for the system.

b. An externally addressable programmable read-only memory (PROM) to provide channel number, sequence, and type control.

c. A digital control bus which allows digital data cards to be inserted in any card slot or several digital data channels to be placed on the same circuit card.

No CMOS compatible or other low power consumption PROMs were available for use on the VPR. Therefore, it was necessary to use standard fuseable link bipolar PROMs. In normal use, these PROMs are not CMOS compatible and have a very high power consumption which is not desireable. However, a special pulsed power mode of operation was developed which allows these PROMs to operate at a few-thousandths of their normal power consumption. Low power or pulsed power interfacing was also utilized.

3.1.4 Power Supply Design

Two of the original objectives were to allow for 28 VDC vehicle power or for internal battery power. The use of CMOS electronics and incremental recording ensures low power consumption. A 12-volt, 4.5-ampere-hour rechargeable battery was chosen for use as the system battery. This capacity battery will supply the recorder, the controller, and signal conditioning for 8 hours at the highest sampling rate (longer periods at slower sampling rates are possible). A series regulator circuit was chosen to reduce the 28 VDC vehicle power to 12 volts for charging the battery and operating the electronics. When vehicle power is used, the battery remains in the circuit to reduce the effects of vehicle power system noise upon VPR operation.

3.1.5 Total System Configuration

A block diagram of the complete VPR system is in figure 3.1-2. The specifications for the VPR are:

a. Size: 13 by 17 by 11 inches (33.0 by 43.1 by 27.9 cm).

b. Weight: 15 pounds (6.8 kilograms).

c. Number of Data Channels: Programmable from 1 to 16.

d. Type of data channels: Programmable for analog or digital in any mixture which does not exceed 16 total channels.

e. Sequence of data channels: Programmable to provide any random or sequential scheme of up to 256 steps desired.

f. Program start address: Selected by a switch register to any value between 0 and 256. Thus, many short data acquisition programs may be stored on a single PROM and addressed by the switch register or only a portion of a program may be selected.

3.1.5 (Cont'd)

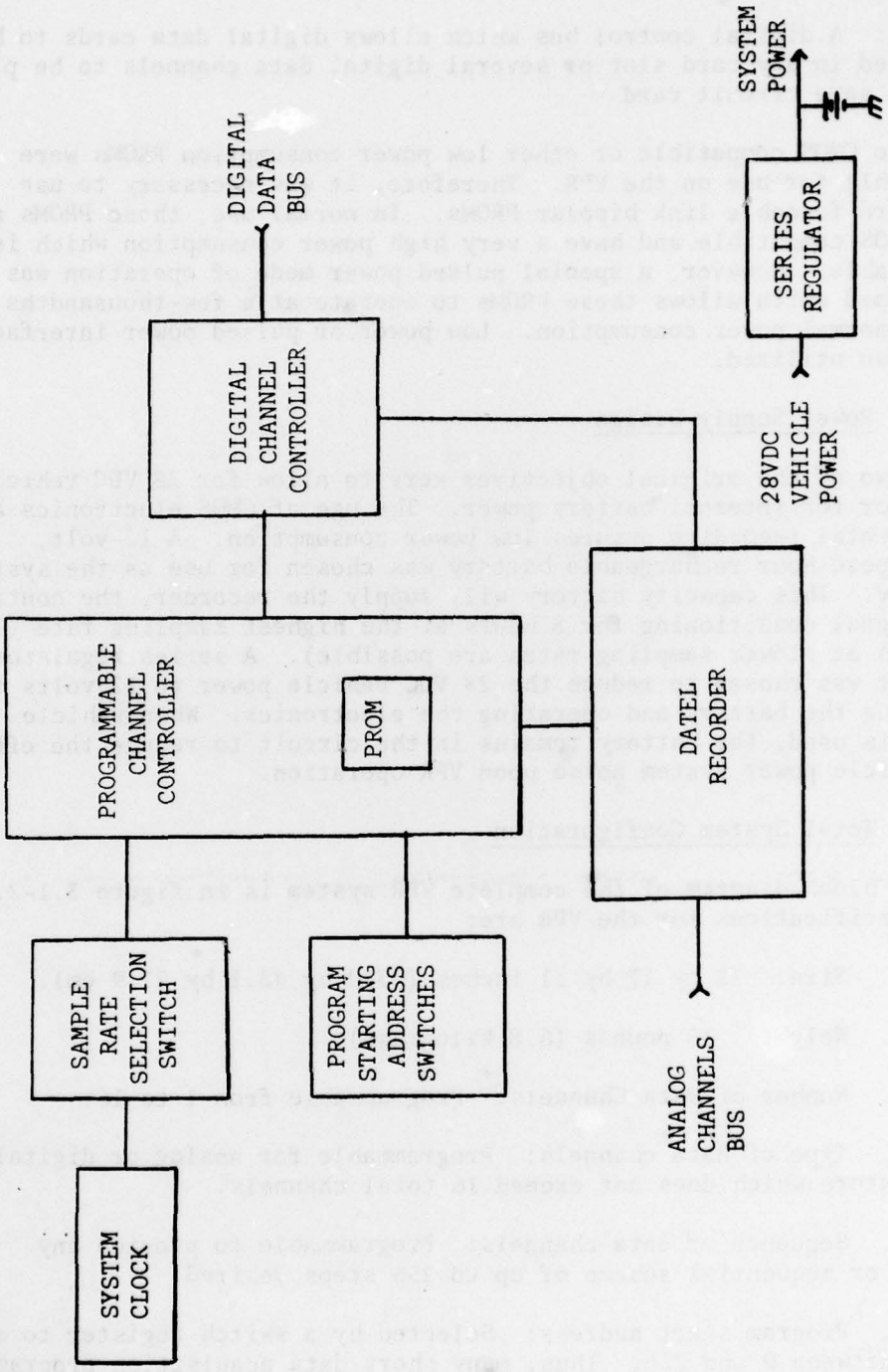


Figure 3.1-2. Block diagram of VPR.

3.1.5 (Cont'd)

g. Data recording rate: Eight switch selectable values from 4 Hz to 0.03125 Hz in binary steps.

h. External power: When used, 18 to 28 VDC at 0.8 amperes maximum.

i. External digital input: Up to 12 bits, positive-true, CMOS compatible data for each channel. A digital formatter circuit is required for each digital channel.

j. External analog input: ±5 volts full scale with ±10 volts maximum overload. Digitized to 12 bit 2's complement format.

A picture of the VPR is in figure 3.1-3.

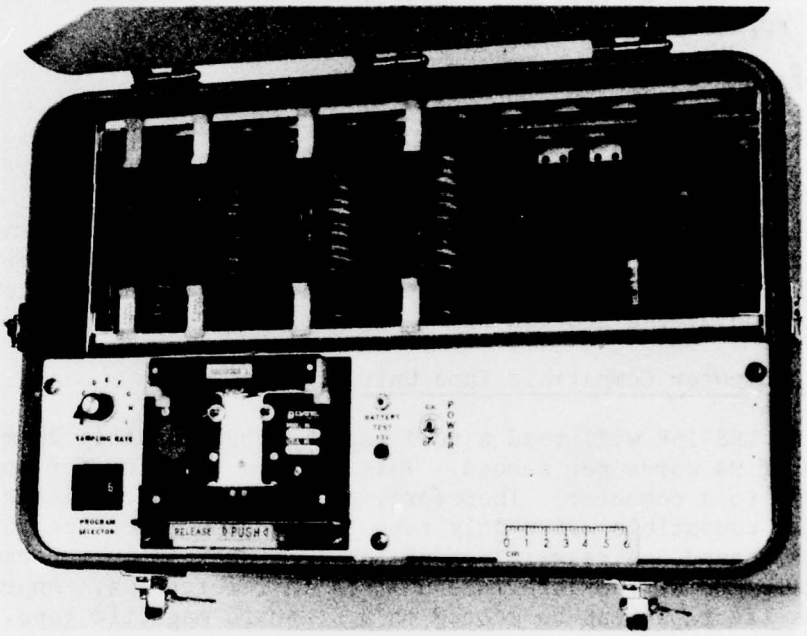


Figure 3.1-3. Vehicle performance recorder.

Operation of the VPR involves the following steps:

a. Determine the channel type, number, and sequence.

b. Install the appropriate digital and analog input circuit cards in the VPR.

c. Program the PROMs with this control sequence and install in the VPR.

d. Set the data recording rate switch and the PROM start address to the appropriate values.

e. Install the VPR on the vehicle.

f. Connect the vehicle transducers to the VPR.

g. Insert a cassette tape cartridge in the VPR recorder.

h. Turn the VPR on when ready to take data.

i. When cassette is full or test is finished, turn off power and remove cassette.

With the exception of the recorder, all circuitry was designed and fabricated in-house. A system interconnection diagram, schematic diagrams, detailed circuit description, and PROM programming instructions are in appendix B.

3.2 PLAYBACK SYSTEM DESIGN

3.2.1 Cassette Reader

A special cassette tape reader is required to read the data from the tape. A Datel LPS-16R was purchased for this requirement. The LPS-16R reads the data off the tape, formats it into a 16-bit word, and provides a word sync pulse when the data is valid. A complete description of the LPS-16R is contained in reference 2.

3.2.2 Computer Compatible Tape Unit

The LPS-16R will read a full tape in approximately 20 minutes at a rate of 94 words per second. This rate is too slow for connection directly to a computer. Therefore, a 9-track, 800-character per inch, computer compatible write-only tape deck and an interface to the LPS-16R were purchased. A description of the tape deck is in reference 3 and a description of the interface unit is in reference 4. Approximately 80 cassette tapes can be stored on a standard magnetic tape.

The procedure for transferring data from the cassette to the standard tape is:

a. Mount the standard cassette tapes and set to load point.

b. Set the header switches on the interface unit to the desired header.

c. Press the run button.

d. When the transfer is completed, the unit will automatically shut off.

e. The cassette can be removed and another cassette loaded for transfer to the same standard tape.

A picture of the playback system is in figure 3.2-1.

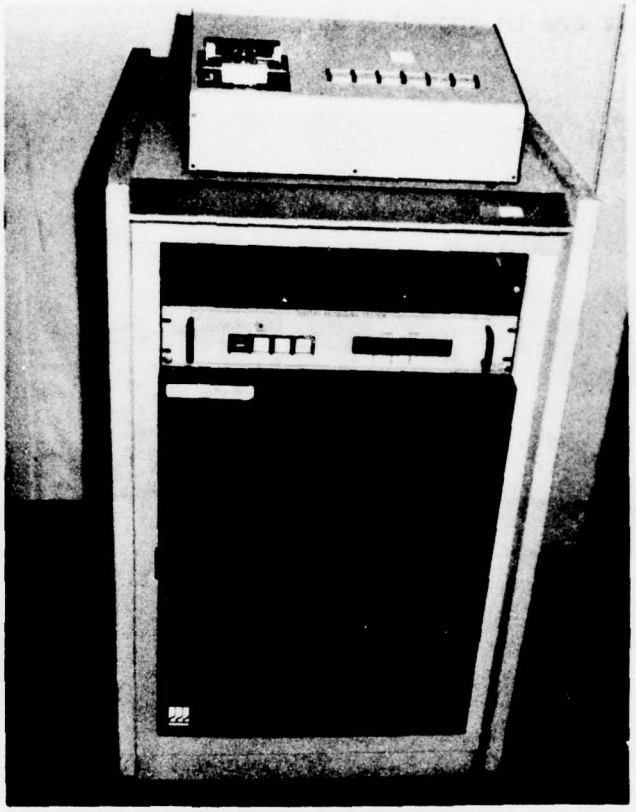


Figure 3.2-1. VPR playback system.

3.2.3 Readout Unit

The computer compatible tape unit is useful once the system has been fully checked out. However, during initial setup and testing, the sequence is too time consuming for efficient field use. For this reason, a separate readout unit which connects directly to the LPS-16R was developed. The readout unit contains a channel address display and a data display along with a push button to advance the tape one word at a time. The channel address display provides the decimal channel number (0-15). The data display provides a decimal number in the range -2048 to +2047 which must be multiplied by a scale factor to convert to the actual input units. The unit contains no memory or word counter so it is not useful for long data searches. But it does

provide sufficient information to allow checking that the correct PROM program is operational and that the input tranducers and signal conditioning are working properly.

A picture of the readout unit is in figure 3.2-2. Details of the readout unit are in appendix D.

Figure 3.2-2. VPR readout unit.

3.2.4 Calculator Interface

During the field testing of the VPR, it became apparent that a faster turn around and more flexible processing technique were desirable. To achieve these goals the LPS-16R was interfaced to a Hewlett-Packard 9825 calculator. This interface allows data to be read from the cassette tape into the calculator memory for immediate processing and analysis.

Details of the calculator interface are in appendix E.

3.3 DATA INTEGRITY TEST

A major problem with digital recording is that a single bit error in a word can drastically change the value of the digital word. Generally, parity checks and/or read after write techniques are applied

to reduce the effect of errors. However, the LPS-16 does not employ any of these techniques. The manufacturer specifies the bit error rate of the LPS-16 and LPS-16R as 1 bit in 10^7 each while the remainder of the playback system is rated at 2 bits in 10^7. For the entire system the bit error rate is roughly 1 error per full cassette.

A test was conducted to determine if the actual error rate agreed with this value. The test was carried out by placing a known voltage at the analog input to the VPR. The system was allowed to record until the cassette was full or nearly full. The data on the cassette was transferred to a standard tape using the playback system. A computer program then examined the data to determine that the channel address and data value were as expected.

In general, the last word on a file was in error. This occurs because when the recorder is shut off or runs out of tape it may be in the middle of recording a word. The word is truncated which results in the error. These errors were not counted as bit errors.

Occasional errors in the first word or two on a file were found. These errors appear to be the result of loose tape. These errors were not counted as bit errors. Based on these observations, the first and last words on a file should be disregarded.

In addition to the errors at the beginning and end of a file three words were found to be in error out of 710,070 total words recorded. The difference between the words with errors and the correct words was examined. None of the errors resulted from a single bit error, but rather from multiple bit differences with shifts of the entire word. Thus, the errors appear to result from a hardware malfunction or tape imperfections longer than one word.

An additional test was carried out with the VPR mounted on a shaker to simulate vibration during data acquisition. A 17.5 Hz sinusoidal waveform at a 1 g level was applied (separately, not simultaneously) to the x, y, and z axis of the VPR. No errors above what was expected from the nonvibrational tests were found.

3.4. EXAMPLES

3.4.1 Time In Gear

For this test a switch plate was attached to the gear shift of an M35 truck. The switches activated logic circuitry on a signal conditioning card located in the VPR which provided a digital word for recording. A thumbwheel switch operated by the driver was also included to allow coding the particular test course in use. The switches were sampled at the rate of once per second.

3.4.1 (Cont'd)

Analysis was carried out on the 9825 calculator. A program was written which counted the number of times a gear was used and the amount of time spent in a particular gear. A sample of the program output is in figure 3.4-1

Date: 9 February 1979 Time: AM
Test: Gear Identification on Vehicle M35AC USA#NK06UU
Course: Churchville Automotive Course
Length of Test: 3.02 hr.

	Low Range	High Range	Unit
First Gear:			
Number Times Gear Used:	0.00	1.00	
Total Time in Gear:	0.00	7.00	sec
% of Course Time in Gear:	0.00	0.12	%
Mean Time in Gear:	0.00	7.00	sec
Deviation:	0.00	0.00	sec
Second Gear:			
Number Times Gear Used:	35.00	2.00	
Total Time in Gear:	1183.50	16.00	sec
% of Course Time in Gear:	10.80	0.14	%
Mean Time in Gear:	33.81	8.00	sec
Deviation:	23.96	2.83	sec
Third Gear:			
Number Times Gear Used:	55.00	4.00	
Total Time in Gear:	3731.00	78.00	sec
% of Course Time in Gear:	34.04	0.72	%
Mean Time in Gear:	67.84	19.50	sec
Deviation:	170.06	13.08	sec
Fourth Gear:			
Number Times Gear Used:	45.00	2.00	
Total Time in Gear:	1275.00	195.00	sec
% of Course Time in Gear:	11.64	1.78	%
Mean Time in Gear:	28.34	97.50	sec
Deviation:	28.94	101.12	sec
Fifth Gear:			
Number Times Gear Used:	44.00	0.00	
Total Time in Gear:	2243.00	0.00	sec
% of Course Time in Gear:	20.46	0.00	%
Mean Time in Gear:	50.98	0.00	sec
Deviation:	44.77	0.00	sec
Reverse:			
Number Times Gear Used:	1.00	0.00	
Total Time in Gear:	16.00	0.00	sec
% of Course Time in Gear:	0.30	0.00	%
Mean Time in Gear:	16.00	0.00	sec
Deviation:	0.00	0.00	sec
Neutral Gear:			
Number Times in Gear:	27.00		
Total Time in Gear:	2124.00		sec
% of Course Time in Gear:	19.38		%
Mean Time in Gear:	78.67		sec
Deviation:	151.21		sec

Figure 3.4-1. Sample of program output for time in gear test.

3.4.2 Vehicle Data

For this test an M151 vehicle was instrumented to measure speed, rpm, battery voltage, brake use, engine temperature, and engine oil pressure. Speed, rpm, and brake use were processed in a digital format by the signal conditioning cards. The other parameters were processed in an analog format. The data rate was two samples per second.

Analysis was carried out on the 9825 calculator. A program was written which processed the raw data to convert it to engineering units, find maximum, minimum, and average values, and plot or list the results. A sample of the program output is in figure 3.4-2. Plots of a portion of a test are in figure 3.4-3.

```
                        VPR ROAD TEST

Test: No. 2                          Date: 23 August 1978
% of Time in Motion: 99.62 %

SPEED
  Maximum:    45.74   mph          Mean:          32.59   mph
  Minimum:     0.00   mph          Deviation:     10.60   mph
  % above   40   mph: 20.20        % below   25   mph: 18.30

RPM
  Maximum: 2700.00   rpm          Mean:        1972.73   rpm
  Minimum:    0.00   rpm          Deviation:    360.00   rpm
  % above 5000   rpm:  0.00        % below 2000   rpm: 43.50

OIL PRESSURE
  Maximum:    41.62   lbs          Mean:          37.41   lbs
  Minimum:     0.00   lbs          Deviation:      1.46   lbs
  % above   38   lbs: 27.10        % below   35   lbs:  4.96

ENGINE TEMPERATURE
  Maximum:    70.19 deg C          Mean:          61.84 deg C
  Minimum:    20.00 deg C          Deviation:      4.94 deg C

BATTERY VOLTAGE
  Maximum:    29.11 volts          Mean:          27.36 volts
  Minimum:    25.86 volts          Deviation:      0.24 volts

BRAKE USAGE
  Number times used: 13            Mean Duration: 4.83 sec
  % time used: 0.03                Deviation:     0.03 sec
```

Figure 3.4-2. Sample of program output for six channels of vehicle data.

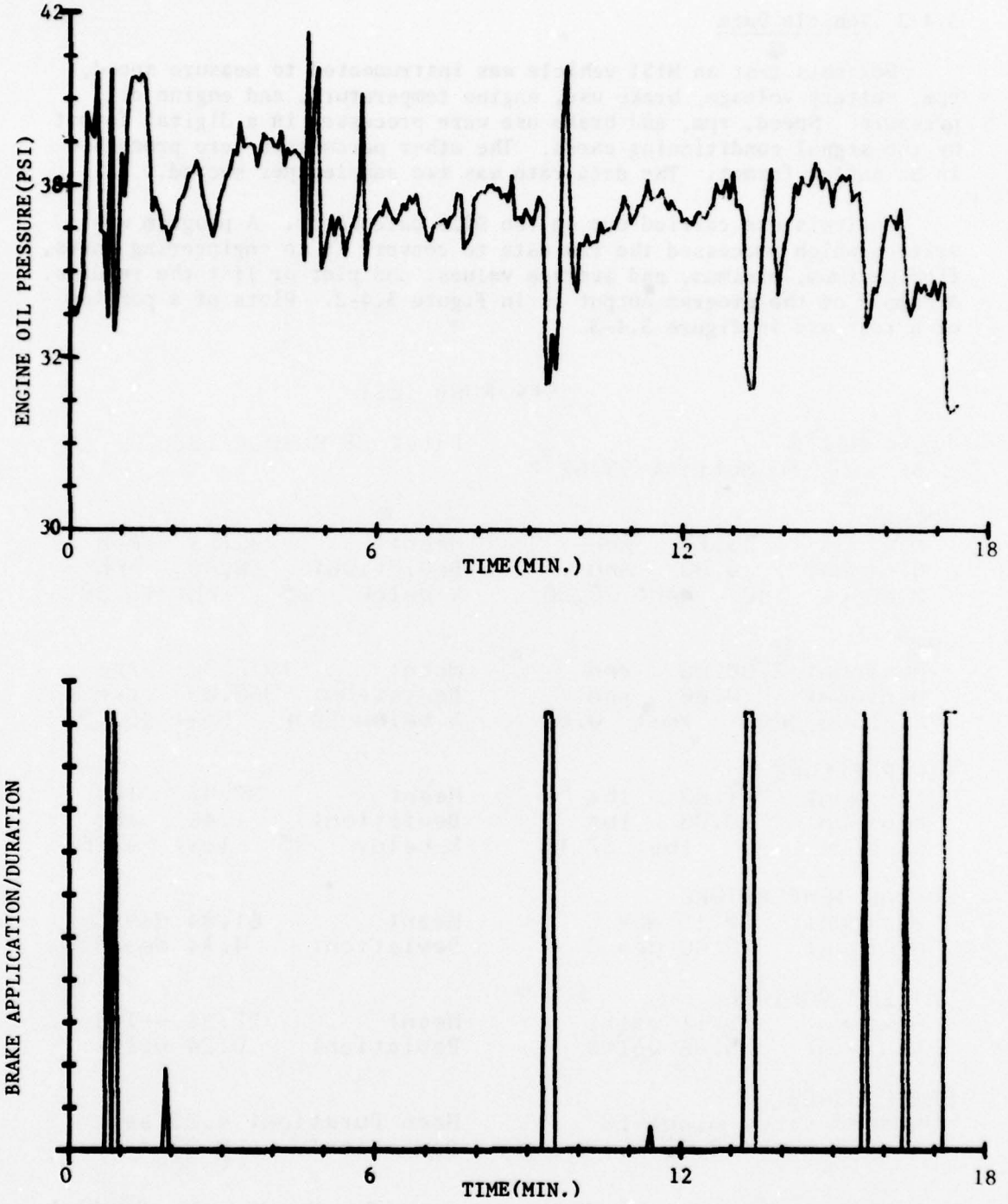


Figure 3.4-3. Sample plots of six channels of vehicle data.

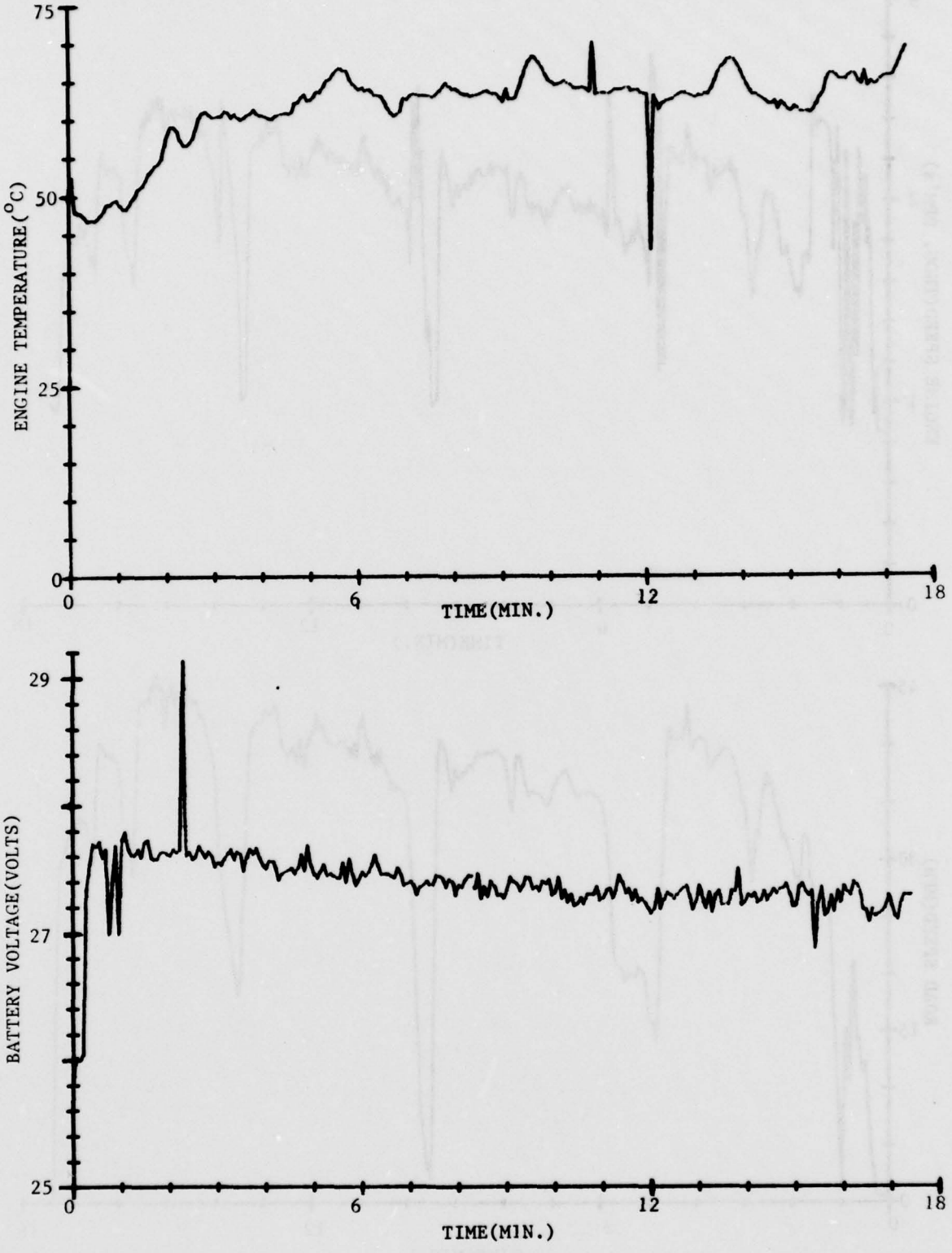
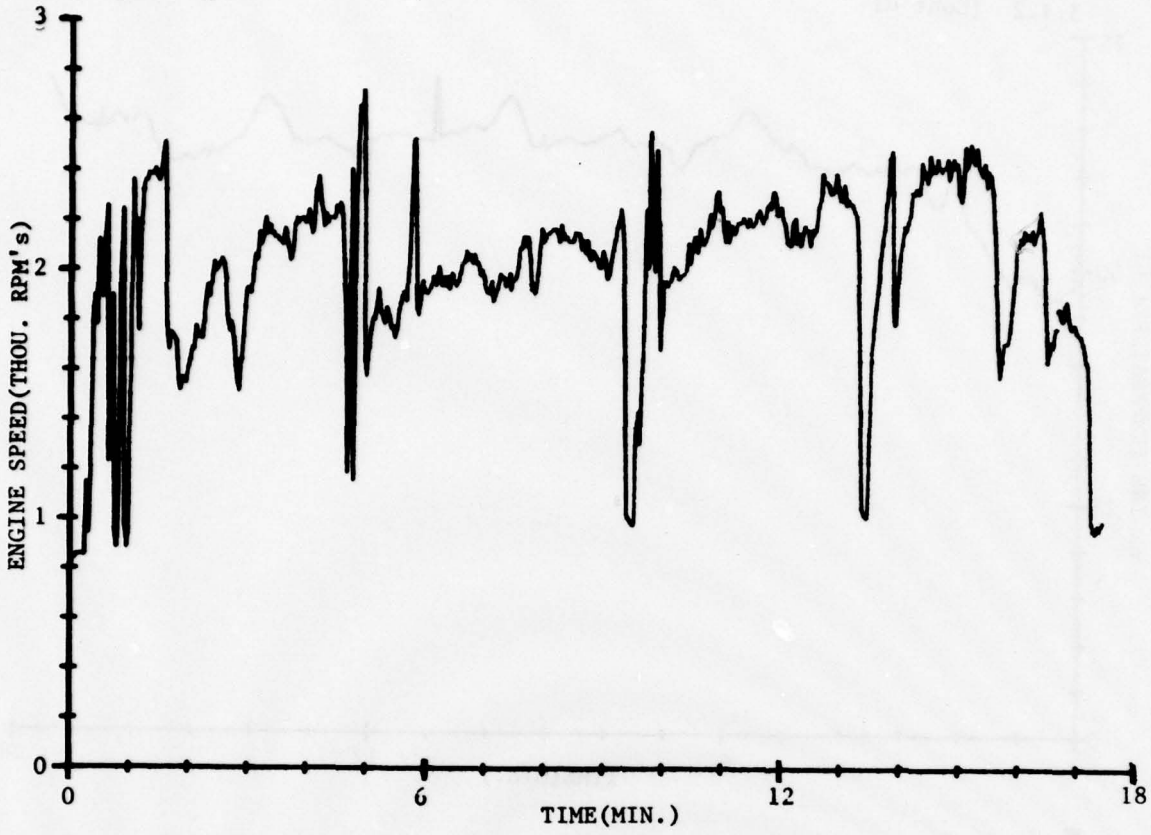


Figure 3.4-3. Continued.

3.4.2 (Cont'd)



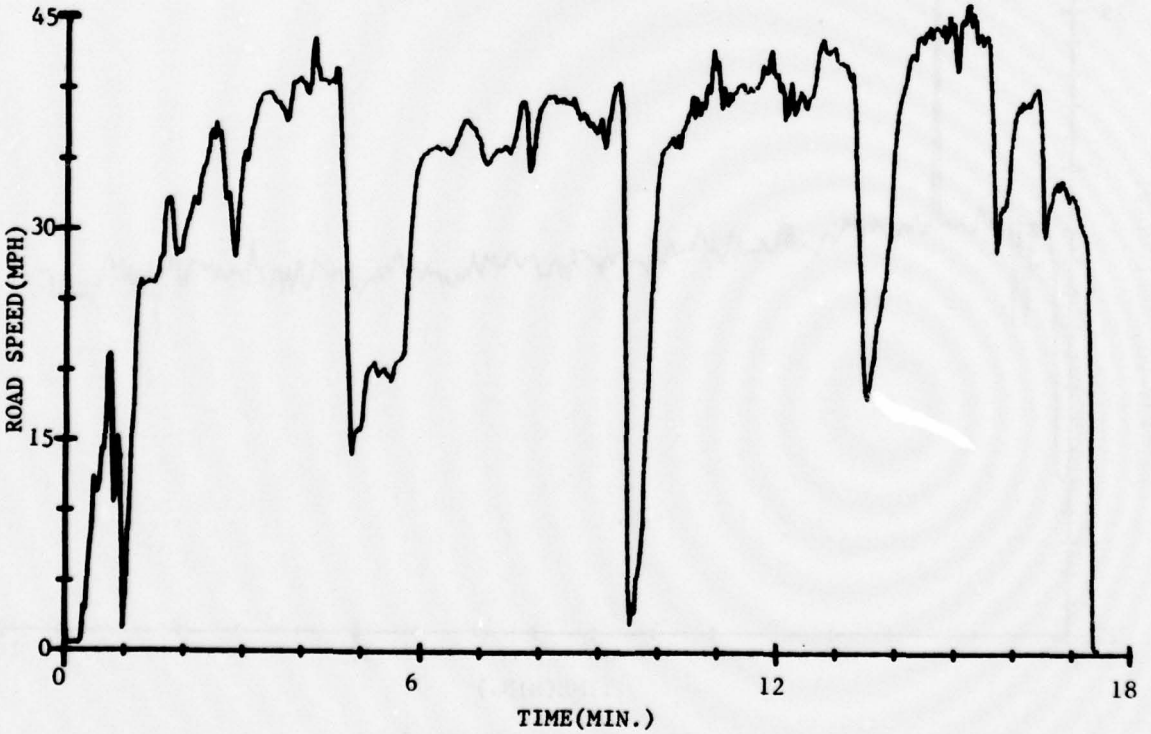


Figure 3.4-3. Continued.

3.4.3 Long-Term Unattended Operation

As an example of the long-term unattended data collection capability of the VPR, two analog temperature channels were recorded over a 4.5-day period. One recorded the indoor temperature and the other the outdoor temperature at building 370. The sample rate was one channel every 32 seconds. Data collection was automatic once the VPR was started. The plot is in figure 3.4-4.

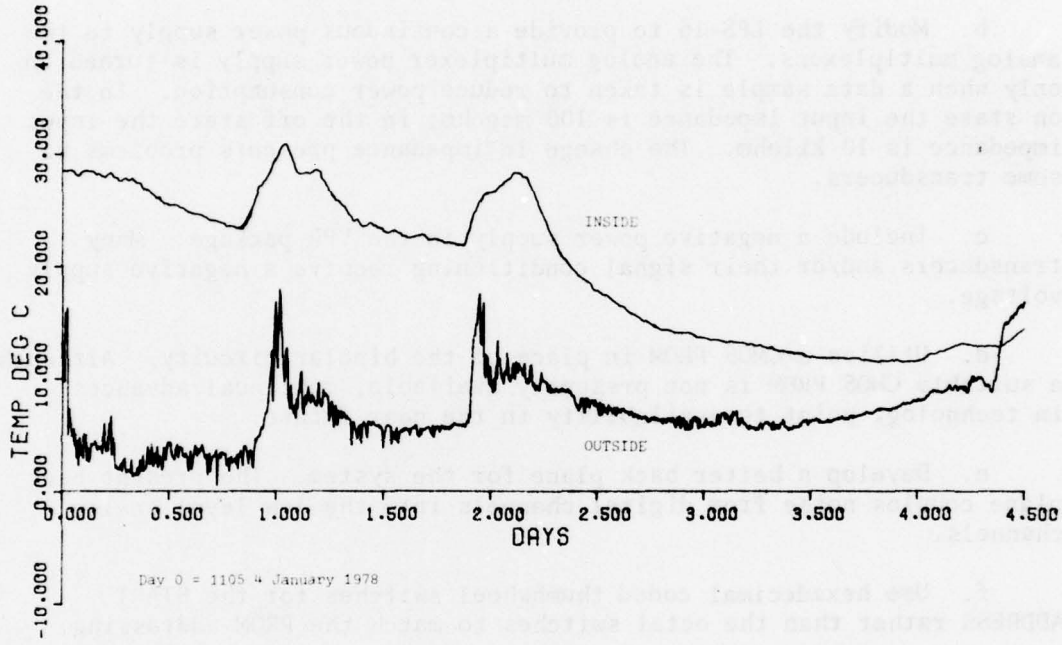


Figure 3.4-4. Plot of temperature data collected on VPR.

3.5 RECOMMENDED MODIFICATIONS

During the testing of the VPR several deficiencies were discovered in the system. If additional systems were to be built, modification of the VPR to correct these problems would be advantageous. The suggested modifications are:

a. Use a 16 VDC battery for internal power with an additional series regulator to provide a constant operating voltage for the LPS-16. The offset and gain of the analog input of the LPS-16 are a function of supply voltage. The internal battery voltage changes with time resulting in some inaccuracy in analog voltage measurement.

b. Modify the LPS-16 to provide a continuous power supply to the analog multiplexers. The analog multiplexer power supply is turned on only when a data sample is taken to reduce power consumption. In the on state the input impedance is 100 megohm; in the off state the input impedance is 10 kilohm. The change in impedance presents problems to some transducers.

c. Include a negative power supply in the VPR package. Many transducers and/or their signal conditioning require a negative supply voltage.

d. Utilize a CMOS PROM in place of the bipolar circuity. Although a suitable CMOS PROM is not presently available, continual advances in technology point to availability in the near future.

e. Develop a better back plane for the system. The present back plane couples noise from digital channels into the low level analog channels.

f. Use hexadecimal coded thumbwheel switches for the START ADDRESS rather than the octal switches to match the PROM addressing.

3.6 COMMENTS

Although the technology utilized at the start of the project was close to the available state-of-the-art, rapid changes in technology have advanced the present state-of-the art. In particular, the development of CMOS microprocessors, low power solid state memory, magnetic bubble memory, and higher density cassette recorders make possible the development of more sophisticated and higher capability data acquisition systems than the present VPR. As a result, a number of commercial manufacturers have introduced products which provide a wide variety of data acquisition configurations. However, most do not have the programming or interfacing flexibility or the digital data handling capability of the VPR. Table 3.6-1 lists several of the commercial systems available. The list is not intended to be inclusive, only to provide a sample of the type of commercial systems available.

3.6 (Cont'd)

TABLE 3.6-1. SAMPLE COMMERCIAL DATA ACQUISITION SYSTEMS

1. A.D. DATA SYSTEMS, INC. - Model ML-10 "Minilogger". 10 analog input channels, 8 bit accuracy; 32 digital input bits; cassette recorder; stand-alone battery operation; real time clock; internal LCD display of time and data; RS-232 output; input range switching; -5° C to +55° C; 8 pounds; 14 X 32 X 30 cm (HWD).

2. DATEL SYSTEMS, INC. - Model DL-2 Datalogger - 64 analog input channels, 12 bit accuracy, 36 digital input bits; cassette recorder; stand-alone battery operation; real time data clock; -20° C to +70° C; 20 pounds; 31 X 31 X 25 cm (HWD).

3. DIGALOG SYSTEMS INC. - Model DLI 203 - Data Acquisition/Record/Playback System - up to 128 analog input channels, 12 bit accuracy; 16 digital input bits; cassette or nine track tape recorder; real time clock; keyboard and display; RS-232 output; sample rate over 1,000 per second; microprocessor control; flexible programming; 100 pounds; 75 X 49 X 36 cm (HWD).

4. DYNATECH MICROSYSTEMS - Model 6201/6205 - Microprocessor/Cassette Data System - up to 128 analog input channels, 10 bit accuracy; 32 digital input bits; cassette recorder; real time clock; LED display of time and data; RS-232 output; input range switching; microprocessor control; 35 pounds; 28 X 49 X 41 cm (HWD).

5. ELECTRO/GENERAL CORP. - Model 401 "Datamyte" - One analog input channel, 8 bit accuracy; 3 totalize inputs; solid state memory (battery backup); run time clock; RS-232 output; microprocessor control; -40° C to +60° C; 5 pounds; 8 X 19 X 19 cm (HWD).

6. MTS SYSTEMS CORP. - Portable Data Analyzer - 8 analog input channels, 12 bit accuracy; cassette recorder; solid state memory (battery backup); RS-232 output; keyboard and display; microprocessor control; -28° C to +49° C; 35 pounds; 26 X 46 X 31 cm (HWD).

7. ROCKWELL INTERNATIONAL - Tripmaster Instrumentation System - A complete system including sensor set (36 parameters available) microprocessor based data acquisition unit (solid state memory), data retrieval unit (cassette), and software package. Designed specifically for automotive applications.

8. ROCKWELL INTERNATIONAL - Tripmaster Trip Recording System - A complete system to monitor road speed and engine speed plus one other parameter including sensor set, microprocessor based data acquisition unit (solid state memory), data retrival unit (cassette), and software package. Designed specifically for automotive applications.

In addition, the US Army Tank-Automotive Research and Development Command (TARADCOM) has supported a $1 million contractor development effort for a Vehicle Monitoring System (VMS). The VMS includes a sensor set, a microprocessor based data acquisition system, data transfer unit, and a software package. VMS is designed to provide use, condition and maintenance information on a vehicle in the field. Initially, the VMS is targetted for the M35A2 and M113A1 vehicles. A single prototype has been constructed and is presently undergoing evaluation at APG. The VMS is similar in concept to unit 7 of table 3.6-1 except that it is specifically designed to meet the requirements of military vehicle evaluation. However, a decision to begin production on VMS is probably 1 year away with projected delivery at least 2 years away. Final cost and availability to APG is unknown.

The cost of additional copies of the VPR is estimated to be $2,500 for parts and 240 man-hours for assembly (single copies).

4. CONCLUSIONS

It is concluded that:

a. The VPR provides a flexible data acquisition system which satisfies a wide variety of measurement requirements.

b. A number of commercially manufactured units with a wide spectrum of capabilities also exists.

c. The army-developed VMS may possibly be available in the future.

d. No single unit satisfies all possible data acquisition problems.

5. RECOMMENDATION

It is recommended that a commercial design of programmable vehicle performance recorder be procured in a quantity and configuration that will satisfy proving ground measurement needs.

SECTION 2. APPENDICES

APPENDIX A - REFERENCES

1. "LPS-16 Cassette Data Logger Instruction Manual," Document Number LPSBM01401, Datel Systems, Inc., Canton, MA.

2. "LPS-16R Interface Manual," Datel Systems, Inc., Canton, MA.

3. "1300/1500 Operation and Maintenance Manual," Digi-Data Corporation, Jessup, MD.

4. "Digital Recording System Technical Manual QSI Model 108," Quad Systems, Inc., Rockville, MD.

5. "Series 90 Prom Programmer Operating Manual," PRO-LOG Corportation Monterey, CA.

(Page A-2 Blank)

APPENDIX B - DETAILS OF VPR HARDWARE

CONTROL CARD 1 DESCRIPTION

Control card 1 generates the system clock and system timing signals. A block diagram of the circuitry on control card 1 is in figure B-1.

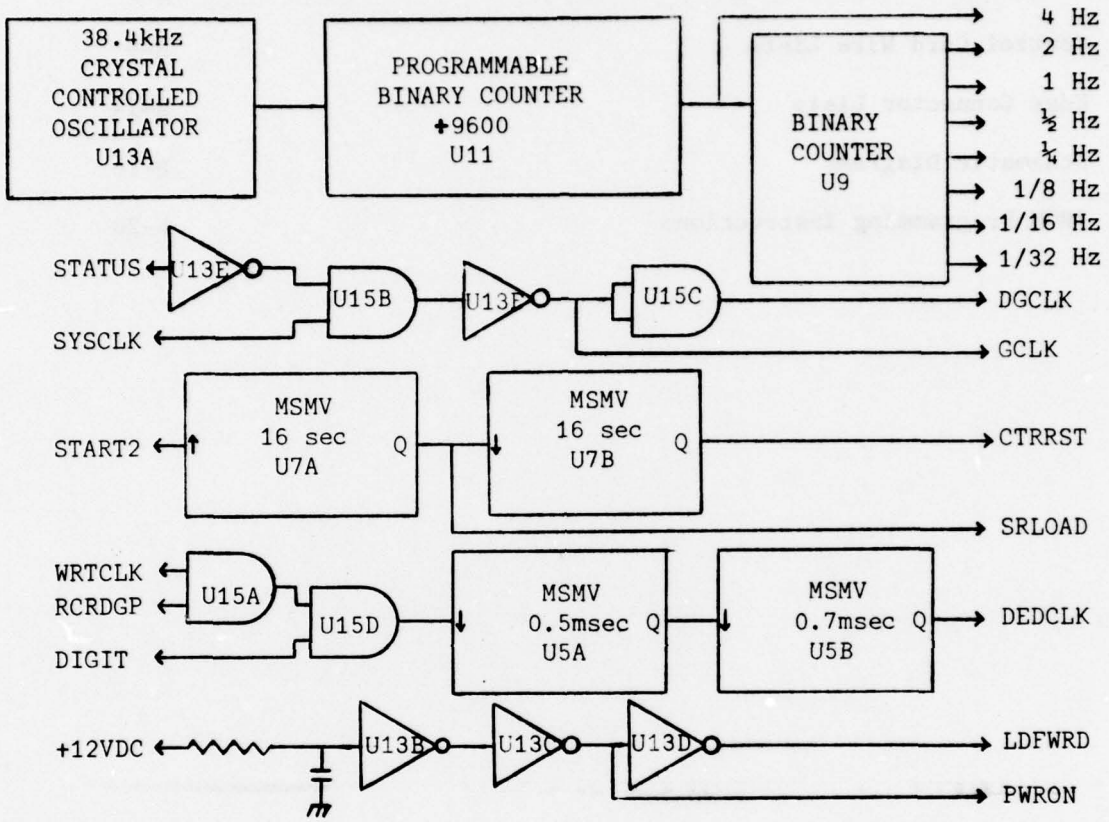


Figure B-1. Block diagram of control card 1 circuitry.

U13A forms the active element of a 38.4 kHz crystal controlled oscillator. U11 is a programmable binary counter which divides the clock by a factor of 9,600 to generate the basic 4Hz system clock. By changing the programming pins of U11 other clock frequencies can be obtained. The 4Hz clock is divided in binary increments by U9 to provide seven lower frequency clocks.

U13E, U15B and U13F gate STATUS with SYSCLK to generate GCLK which inhibits a conversion while the LPS-16 is writing a file gap. The propagation delay of U15C is used to delay GCLK to produce DGCLK.

START 2 is an output of control card 2 which initiates the recording of a digital data word. Monostable multivibrator (MSMV) U7A is triggered by the rising edge of START 2 to generate a 16-microsecond pulse SRLOAD. SRLOAD goes to the digital data bus where it is used to load shift registers which transfer digital data from a parallel format into a serial format required by the LPS-16. The falling edge of SRLOAD triggers MSMV U7B which generates another 16-microsecond pulse CTRRST. CTRRST goes to the digital data bus where it is used to reset counters.

WRTCLK and RCRDGP are gated by U15A to produce a set of 16-bit clock pulses. The 16-bit clock is gated with DIGIT by U15D so that the 16-clock pulses are fed to U5A only when digital data is to be recorded. MSMVs U5A and U5B delay the 16 gated clock pulses by 0.5 millisecond to provide DEDCLK. DEDCLK is used as a clock for the shift registers on digital data cards.

An R-C time constant combined with U13B and U13C generate a 10-second pulse PWRON which is inverted by U13D to generate LDFWRD. LDFWRD goes to the LPS-16 to load forward the cassette tape to eliminate slack. PWRON resets the presettable counters on control card 2.

All inputs to contol card 1 are pulled up to the positive power supply by 120-kilohm resistors.

Control card 1 was wire-wrapped on a Cambion 715-1005-01 type card. Component carriers were utilized to mount discrete components.

CONTROL CARD 2 DESCRIPTION

Control card 2 generates the channel addresses and control signals necessary to operate the LPS-16. A block diagram of the circuitry on control card 2 is in figure B-2.

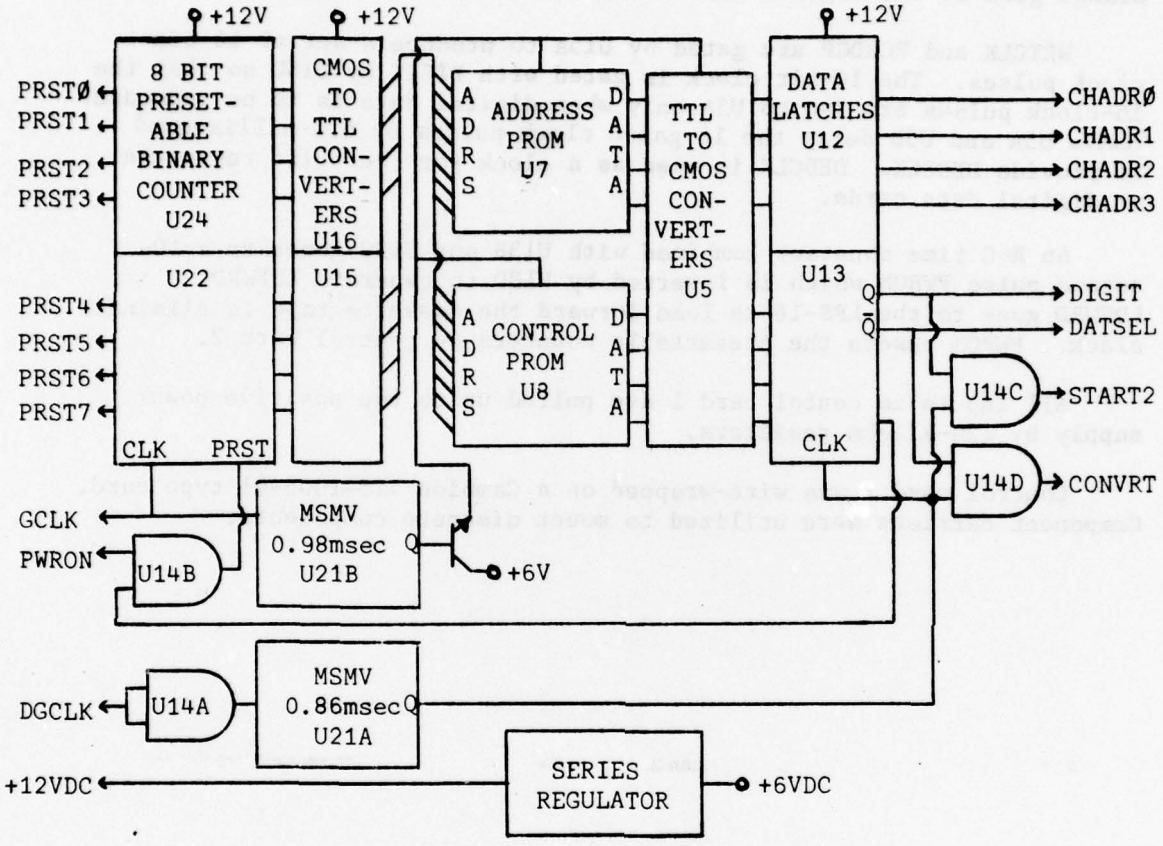


Figure B-2. Block diagram of control card 2 circuitry.

U22 and U24 are connected as an 8-bit presettable binary counter. PRSTØ through PRST7 are the preset lines which are connected to the front panel start address switches. PWRON or an internal preset are gated by U14B to initialize the counter to the values on the preset lines. The counter is incremented by GCLK.

The output lines of the counter go to U15 and U16 where the CMOS levels are converted to transistor-transistor logic (TTL) levels required by PROM's U7 and U8.

U7 and U8 are bipolar fuseable link PROMs organized in a 256-word by 4-bit structure. All inputs and outputs are TTL compatible. The 8 bits of address required for the 256 words are provided by U15 and U16. U7 stores the 4-bit address required by the LPS-16 analog multiplexer and the digital channels. Only 2 bits of U8 are used for control purposes. One bit selects analog or digital recording and the other bit is used to reset the address counters. The outputs of U7 and U8 are open collector.

The address and control bits are converted back to CMOS levels by U5 which is a TTL hex inverter with open collector outputs.

Since U5, U7, and U8 are bipolar they would normally present a large load on the power supply. However, by turning the power on for only a very short period of time and storing the data into a low-power dissipation CMOS data latch, the total power dissipation can be kept small. GCLK triggers MSMV U21B to generate a 1-millisecond pulse which turns on power to U5, U7, and U8.

The outputs of U5 are stored in CMOS data latches U12 and U13. The clock which strobes the data into the latches is provided by U14A and U21A. The U14A provides an additional delay in DGCLK which triggers MSMV U21A to generate a pulse shorter in length than that produced by U21B. The delay introduced by U14A and the shorter pulse generated by U21A guarantee that the data strobed into U12 and U13 is valid. A timing diagram of the pulse relationships is in figure B-3.

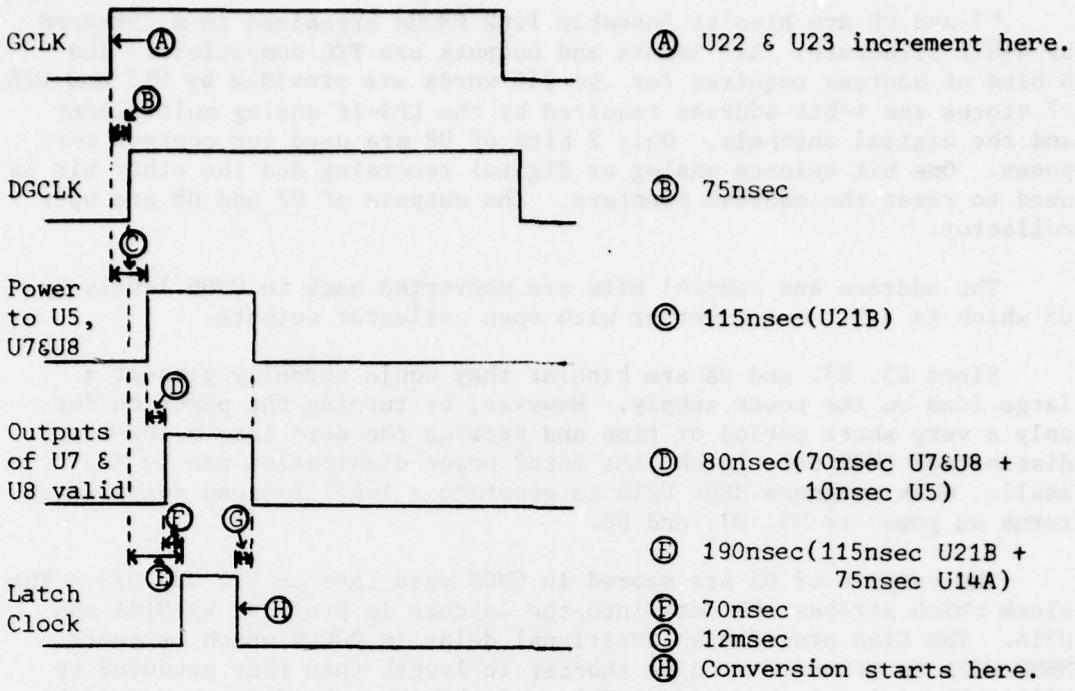


Figure B-3. Control card 2 timing diagram.

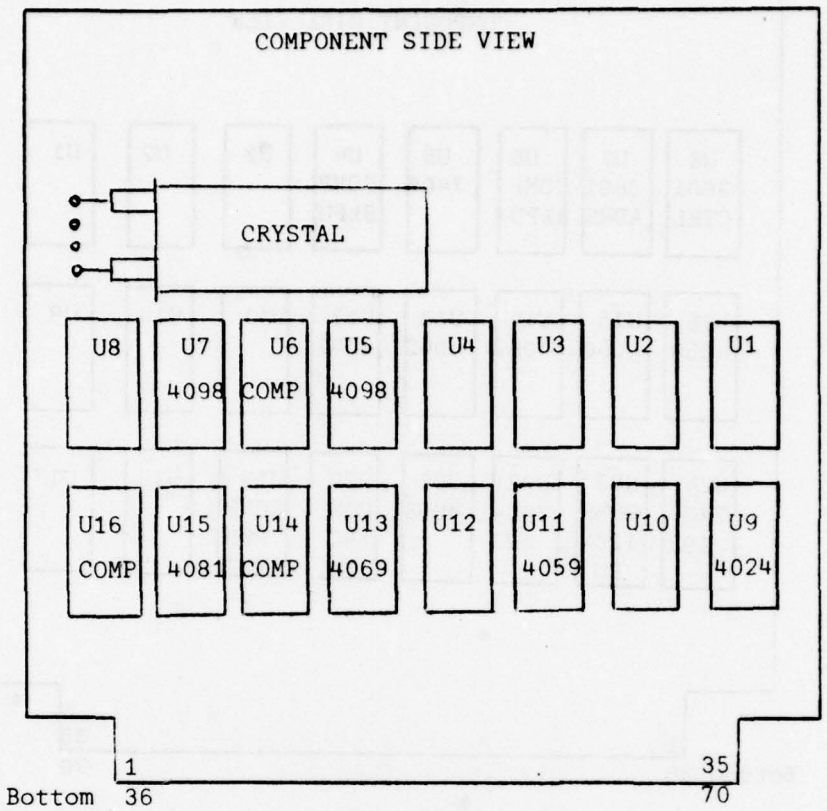
The analog/digital control bit of U13 is gated with the output pulse of U21A in U14C or U14D to generate a digital (START 2) or analog (CONVRT) conversion pulse.

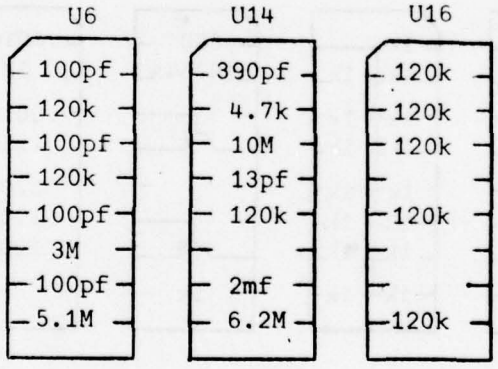
A series regulator is used to produce the +6VDC required by U15, U16, U5, U7, and U8.

Inputs PRSTØ through PRST7 are pulled down to power supply ground by 120-kilohm resistors. All other inputs are pulled up to the positive power supply by 120-kilohm resistors.

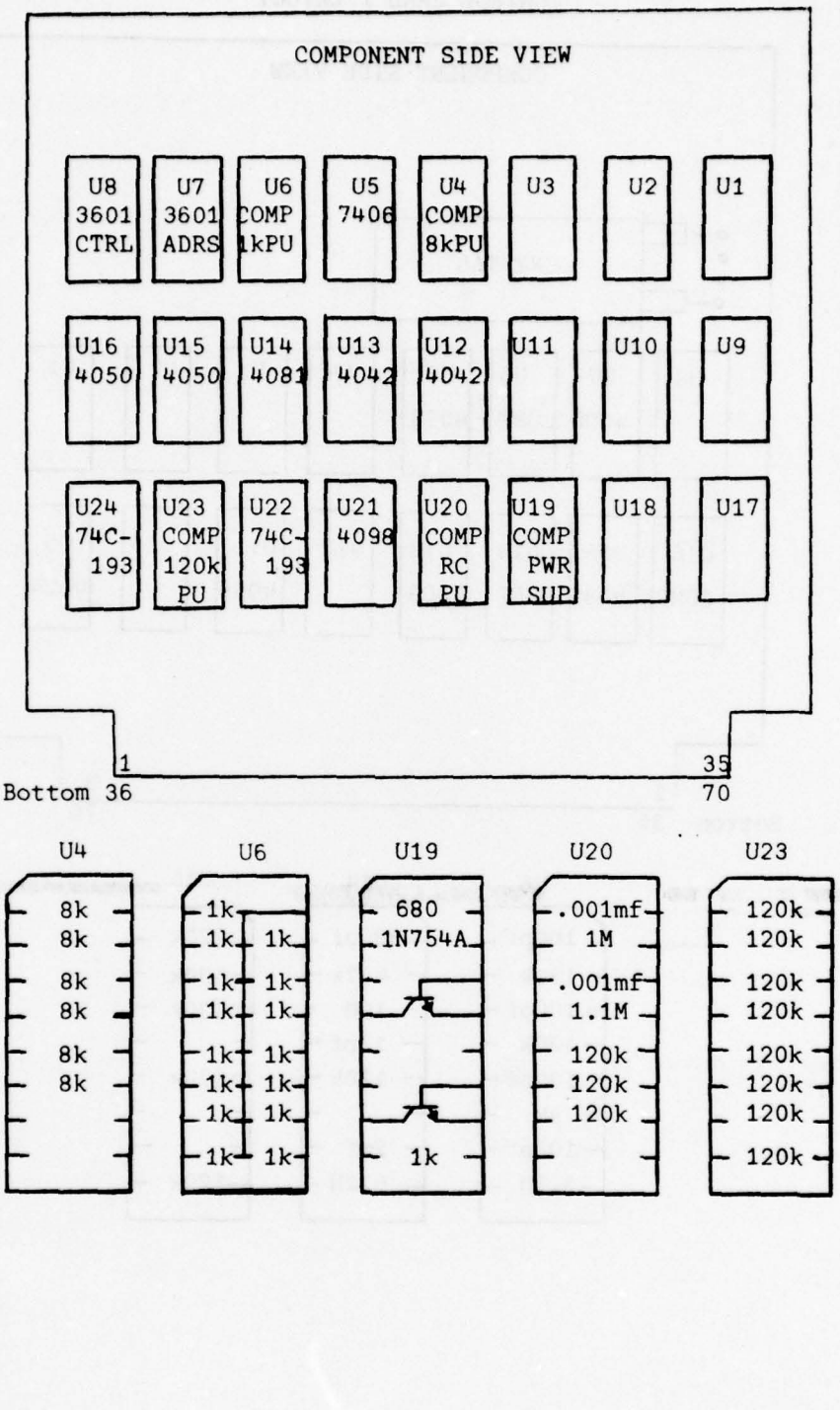
Control card 2 was wire-wrapped on a Cambion 715-1011-01 type card. Component carriers were utilized to mount discrete components.

CONTROL CARD 1 LAYOUT





CONTROL CARD 2 LAYOUT



CONTROL CARD 1
WIRE LIST

FROM	TO	COLOR
C19	C54	RED
C19	W	
C54	Y	
U5/16	U5/P	
U7/16	U7/P	
U9/14	U9/P	
U12/2	U12/P	
U13/14	U13/P	
U15/14	U15/P	
U5/3	U5/13	
U5/13	U5/16	
U7/3	U7/13	
U7/13	U7/16	
U16/8	U16/5	
U16/5	U16/3	
U16/3	U16/2	
U16/2	U16/1	
U16/1	U16/P	
U6/8	U6/6	
U6/6	U6/4	
U6/4	U6/2	
U6/2	U6/P	
U14/8	U14/5	
U14/5	U14/P	
U10/14	U10/15	
U10/14	U10/6	
U10/6	U10/3	
U10/3	U10/P	

FROM	TO	COLOR
C21	C56	BLACK
C21	X	
C56	Z	
U5/8	U5/G	
U7/8	U15/G	
U9/7	U9/G	
U10/11	U10/G	
U13/7	U13/G	
U15/7	U15/G	
U5/12	U5/4	
U5/4	U5/G	
U7/12	U7/4	
U7/4	U7/G	
U14/7	U14/4	
U14/4	U14/1	
U14/1	U14/G	
U9/2	U9/G	
U10/12	U10/5	
U10/5	U10/2	
U10/2	U10/G	
U11/6	U11/5	
U11/5	U11/3	
U11/3	U11/2	
U11/2	U11/G	
U11/11	U11/14	
U11/14	U11/G	
U12/5	U12/11	
U12/11	U12/12	
U12/12	U12/14	

CONTROL CARD 1
WIRE LIST

FROM	TO	COLOR
U11/12	U11 15	RED
U11/15	U11/P	↓
U5/10	C52	BLUE
U7/6	C38	
U7/10	C40	
U15/10	C42	
U13/12	C45	
U12/3	C70	
U9/12	C69	
U9/11	C68	
U9/9	C67	
U9/6	C66	
U9/5	C65	
U9/4	C64	
U9/3	C63	
U13/8	C49	
U13/6	C48	↓
U14/2	U14/3	CRANGE
U14/2	U13/2	
U14/15	U14/16	
U14/16	A8	
U14/13	U14/14	
U14/14	D8	
U14/13	U13/1	
U13/2	U12/6	
U12/3	U9/1	
U14/9	U14/10	
U14/10	U13/3	
U13/4	U13/5	
U13/6	U13/9	
U13/10	U15/6	
U15/4	U13/13	↓

FROM	TO	COLOR
U12/14	U12/15	BLACK
U12/15	U12/6	
U7/5	C8	GREEN
U15/13	C7	
U15/2	C6	
U15/1	C5	
U15/5	C4	
U13/11	C16	
U16/9	U7/5	
U16/14	U15/13	
U16/15	U15/2	
U16/16	U15/1	
U16/12	U15/5	
U14/12	U13/11	↓
U13/12	U15/9	ORANGE
U15/9	U15/8	
U15/3	U15/12	
U15/11	U5/5	
U5/6	U5/11	
U5/1	U6/5	
U6/11	U6/12	
U6/12	U5/2	
U5/15	U6/7	
U7/10	U6/9	
U6/10	U5/14	
U7/6	U7/11	
U7/1	U6/1	
U6/15	U6/16	
U6/15	U7/2	
U7/15	U6/3	
U6/13	U6/14	
U6/14	U7/14	↓

CONTROL CARD 2
WIRE LIST

FROM	TO	COLOR
C19	C54	RED
C19	W	
C54	Y	
U4/16	U4/P	
U12/16	U12/P	
U13/16	U13/P	
U14/14	U14/P	
U19/1	U19/P	
U20/2	U20/P	
U21/16	U21/P	
U22/16	U22/P	
U23/1	U23/P	
U24/16	U24/P	
U12/6	U12/16	
U13/6	U13/16	
U19/4	U19/1	
U20/12	U20/11	
U20/11	U20/10	
U20/10	U20/4	
U20/4	U20/2	
U21/5	U21/3	
U21/5	U21/11	
U21/11	U21/13	
U21/13	U21/16	
U23/8	U23/7	
U23/7	U23/6	
U23/6	U23/5	
U23/5	U23/4	
U23/4	U23/3	
U23/3	U23/2	
U23/2	U23/1	
U24/4	U24/16	

FROM	TO	COLOR
C21	C56	BLACK
C21	X	
C56	Z	
U5/7	U13/G	
U7/8	U15/G	
U8/8	U16/G	
U12/8	U20/G	
U13/8	U21/G	
U14/7	U22/G	
U15/8	U23/G	
U16/8	U24/G	
U19/2	U19/G	
U21/8	U21/G	
U22/8	U22/G	
U24/8	U24/G	
U7/13	U7/14	
U7/13	U7/8	
U8/13	U5/14	
U8/13	U8/8	
U13/13	U13/14	
U13/14	U13/8	
U15/11	U15/14	
U15/11	U15/8	
U16/11	U16/14	
U16/10	U16/8	
U22/14	U22/8	
U24/14	U24/8	
U19/10	U5/14	YELLOW
U5/14	U7/16	
U7/16	U8/16	
U19/7	U19/13	

CONTROL CARD 2

WIRE LIST

FROM	TO	COLOR
U4/16	U4/15	RED
U4/15	U4/14	
U4/14	U4/13	
U4/13	U4/12	
U4/12	U4/11	
U12/1	C52	BLUE
U12/2	C49	
U12/10	C50	
U12/11	C51	
U13/2	C47	
U13/3	C48	
U14/10	C43	
U14/11	C45	
U24/5	U21/12	ORANGE
U24/11	U22/11	
U22/11	U14/4	
U24/13	U22/4	
U24/12	U22/5	
U24/3	U16/3	
U24/2	U16/5	
U24/6	U16/7	
U24/7	U16/9	
U22/3	U15/3	
U22/2	U15/5	
U22/6	U15/7	
U22/7	U15/9	
U7/1	U8/1	
U7/2	U8/2	
U7/3	U8/3	
U7/4	U8/4	
U7/5	U8/5	
U7/6	U8/6	

FROM	TO	COLOR
U19/13	U15/1	YELLOW
U15/1	U16/1	
U6/14	U5/14	
U14/1	C10	GREEN
U14/1	U20/6	
U14/5	C12	
U14/5	U20/7	
U21/12	C17	
U21/12	U20/5	
U22/15	C5	
U22/15	U23/14	
U22/1	C6	
U22/1	U23/15	
U22/10	C7	
U22/10	U23/13	
U22/9	C8	
U22/9	U23/12	
U24/15	C1	
U24/15	U23/9	
U24/1	C2	
U24/1	U23/16	
U24/10	C3	
U24/10	U23/10	
U24/9	C4	
U24/9	U23/11	
U7/7	U8/7	ORANGE
U7/15	U8/15	
U16/2	U8/5	
U16/4	U8/6	
U16/6	U8/7	
U16/10	U7/4	
U15/2	U7/3	

FROM	TO	COLOR
U15/4	U7/2	ORANGE
U15/6	U7/1	
U15/10	U7/15	
U7/12	U6/1	
U7/11	U6/2	
U7/10	U6/3	
U7/9	U6/4	
U7/12	U5/1	
U7/11	U5/3	
U7/10	U5/5	
U7/9	U5/9	
U8/12	U6/5	
U8/11	U6/6	
U8/12	U5/11	
U8/11	U5/13	
U5/2	U4/1	
U5/4	U4/6	
U5/6	U4/5	
U5/8	U4/4	
U5/10	U4/3	
U5/12	U4/2	
U5/2	U12/4	
U5/4	U12/7	
U5/6	U12/13	
U5/8	U12/14	
U5/10	U13/4	
U5/12	U13/7	
U21/10	U19/8	
U19/9	U19/11	
U19/16	U19/15	
U19/15	U19/14	
U14/2	U14/1	
U14/3	U21/4	
U21/1	U20/1	

FROM	TO	COLOR
U20/15	U20/16	ORANGE
U20/16	U21/2	
U21/15	U20/3	
U20/14	U20/13	
U20/13	U21/14	
U21/6	U13/5	
U13/5	U12/5	
U13/2	U14/13	
U13/3	U14/9	
U14/8	U14/12	
U13/5	U14/12	
U13/10	U14/6	

WIRE WRAP CONVENTIONS

Top of card is ground.
Bottom of card is +12VDC.

RED -+12VDC
BLACK -Ground
YELLOW-+6VDC
ORANGE-On card signals
BLUE -Output lines
GREEN -Input lines

All sockets are 18 pins-one power(P) pin, one ground(G) pin, and 16 IC pins. On sockets where 14 pin IC's are installed, the two extra pins are not counted; so the wire list gives IC pin numbers not socket numbers.

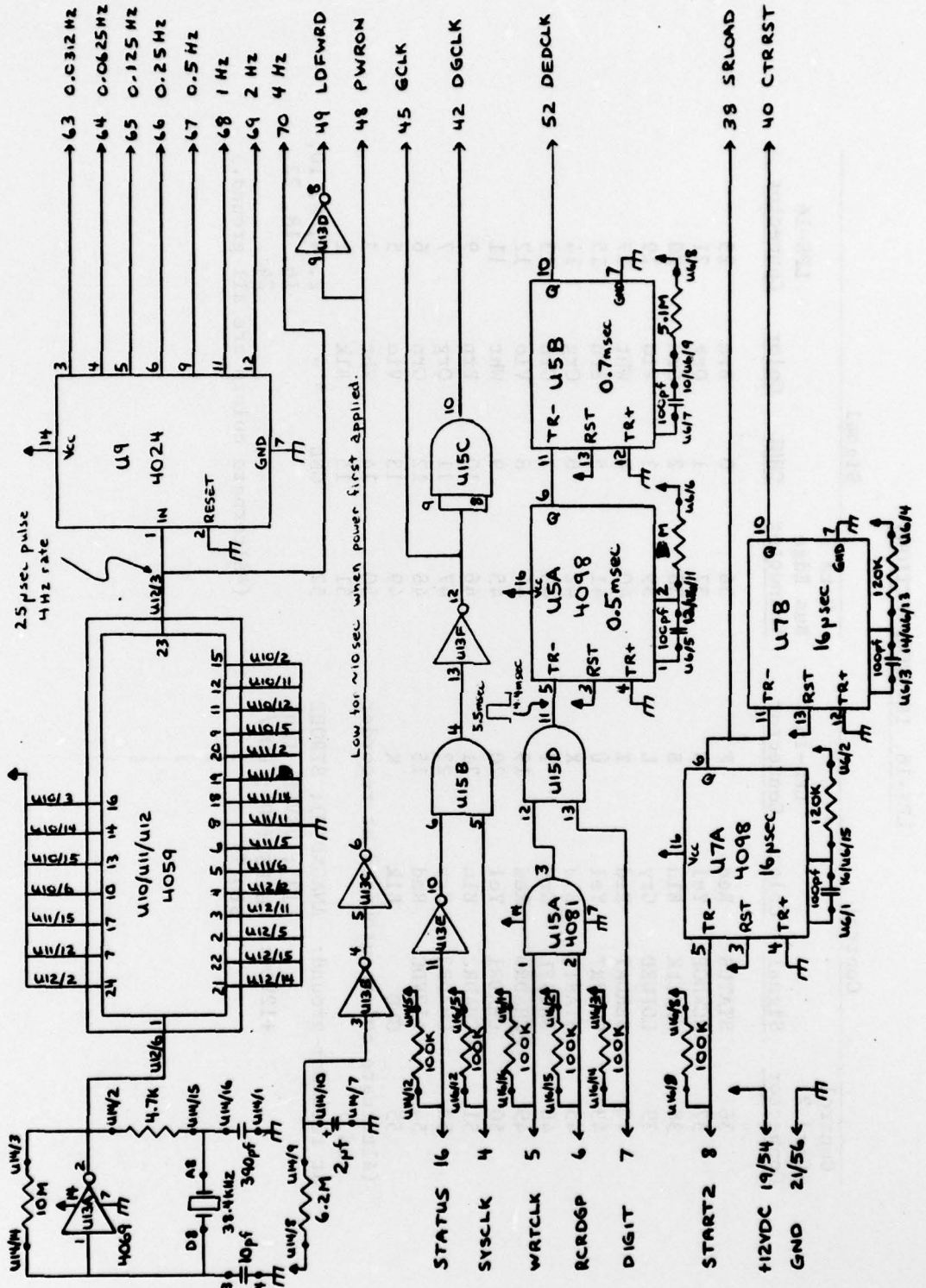
CONTROL CARD 1	EDGE CONNECTOR	CONTROL CARD 2	EDGE CONNECTOR	DATA CARDS EDGE CONNECTOR	
				1-Ch O ANA IN	36-Ch O ANA OUT
1	36	1-PRSTO	36-(STATUS)	2- 1	37- 1
2	37	2-PRST1	37-(RCRDGP)	3- 2	38- 2
3	38-SRLOAD	3-PRST2	38-(WRTCLK)	4- 3	39- 3
4-SYSCLK	39	4-PRST3	39-(LDFWRD)	5- 4	40- 4
5-WRTCLK	40-CTRRST	5-PRST4	40-(SERDAT)	6- 5	41- 5
6-RCRDGP	41	6-PRST5	41	7- 6	42- 6
7-DIGIT	42-DGCLK	7-PRST6	42	8- 7	43- 7
8-START2	43	8-PRST7	43-CONVRT	9- 8	44- 8
9	44	9-(+12VDC)	44	10- 9	45- 9
10	45-GCLK	10-DGCLK	45-START2	11- 10	46- 10
11	46	11	46	12- 11	47- 11
12	47	12-PWRON	47-DIGIT	13- 12	48- 12
13	48-PWRON	13	48-DATSEL	14- 13	49- 13
14	49-LDFWRD	14	49-CHADRO	15- 14	50- 14
15	50	15	50-CHADR1	16- 15	51- 15
16-STATUS	51	16	51-CHADR2	17-ANAGND	52-ANAGND
17	52-DEDCLK	17-GCLK	52-CHADR3	18	53
18	53	18	53	19-+12VDC	54-+12VDC
19-+12VDC	54-+12VDC	19-+12VDC	54-+12VDC	20	55
20	55	20	55-(GND)	21-PWRGND	56-PWRGND
21-GND	56-GND	21-GND	56-GND	22	57
22	57	22	57	23	58
23	58	23	58	24	59
24	59	24	59	25	60
25	60	25	60	26-CHADRO	61
26	61	26	61	27-CHADR1	62
27	62-(SYSCLK)	27	62	28-CHADR2	63
28	63-1/32 Hz	28	63	29-CHADR3	64
29	64-1/16 Hz	29	64	30	65
30	65-1/8 Hz	30	65	31	66
31	66-¼ Hz	31	66	32-DEDCLK	67
32	67-½ Hz	32	67	33-SRLOAD	68
33	68-1 Hz	33	68	34-CNTRST	69
34	69-2 Hz	34	69	35-SERDAT	70
35	70-4 Hz	35	70		

Signals in parenthesis are available on the connector but not used on the board at that pin.

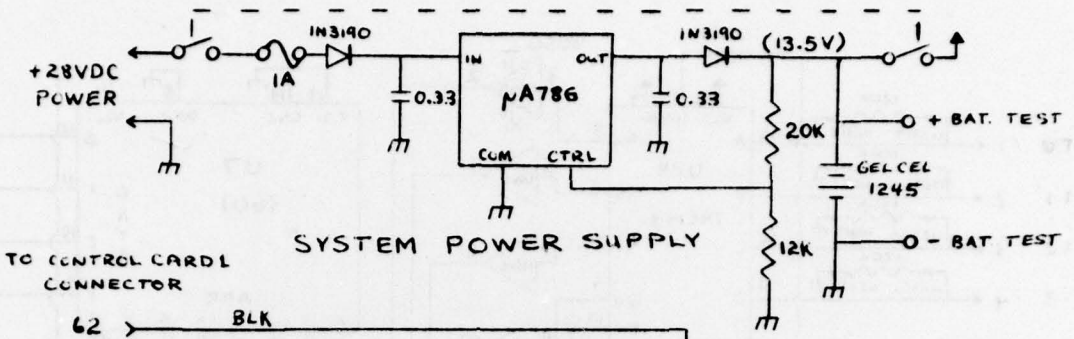
LPS-16 INTERCONNECTIONS

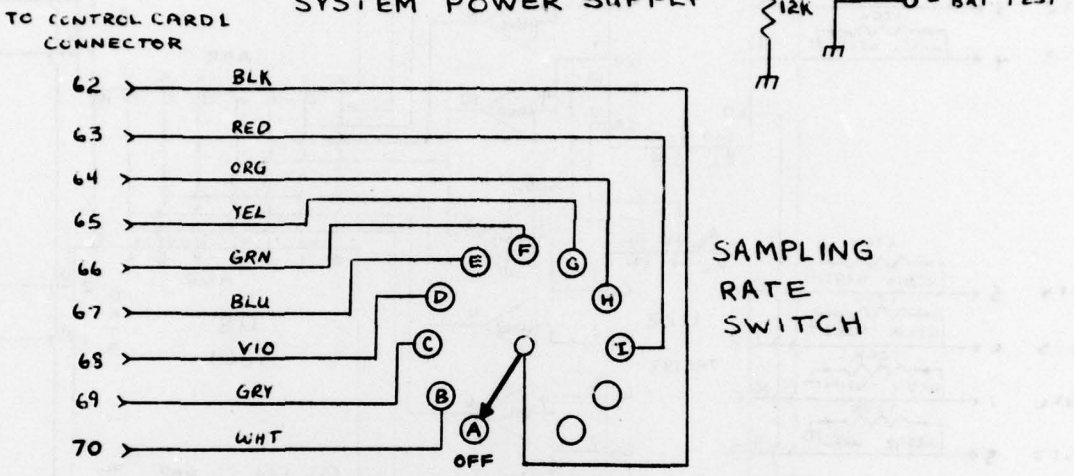
Control				Signal			
Control Card 2 Connector	Signal	Color	LPS-16 Connector	Data Bus Edge Connector	CHNL	Color	LPS-16 Connector
36	STATUS	Red	F	36	0	Brn	23
37	RCRDGP	Yel	N	37	1	Org	21
38	WRTCLK	Blu	B	38	2	Grn	20
39	LDFWRD	Gry	L	39	3	Vio	19
40	SERDAT	Red	Z	40	4	Wht	17
43	CONVRT	Yel	U	41	5	Brn	15
45	START2	Blu	X	42	6	Org	14
48	DATSEL	Gry	Y	43	7	Grn	13
49	CHADR0	Red	19	44	8	Vio	12
50	CHADR1	Yel	20	45	9	Wht	11
51	CHADR2	Blu	21	46	10	Brn	9
52	CHADR3	Gry	22	47	11	Org	7
54	+12VDC	Red	15	48	12	Grn	6
55	GND	Blk	K	49	13	Vio	5
(Alternate colors grounded at recorder end.)				50	14	Wht	3
				51	15	Blk	1
At recorder-ground:		ANAGND(M); STROBE (13); DEVSEL (16)		52	GND	* -	2, 4, 8, 10, 16, 18, 22, 24
+12VDC:		CH1RST(10); RDM/ SEQ(T)		(*Alternate colors are all ground.)			

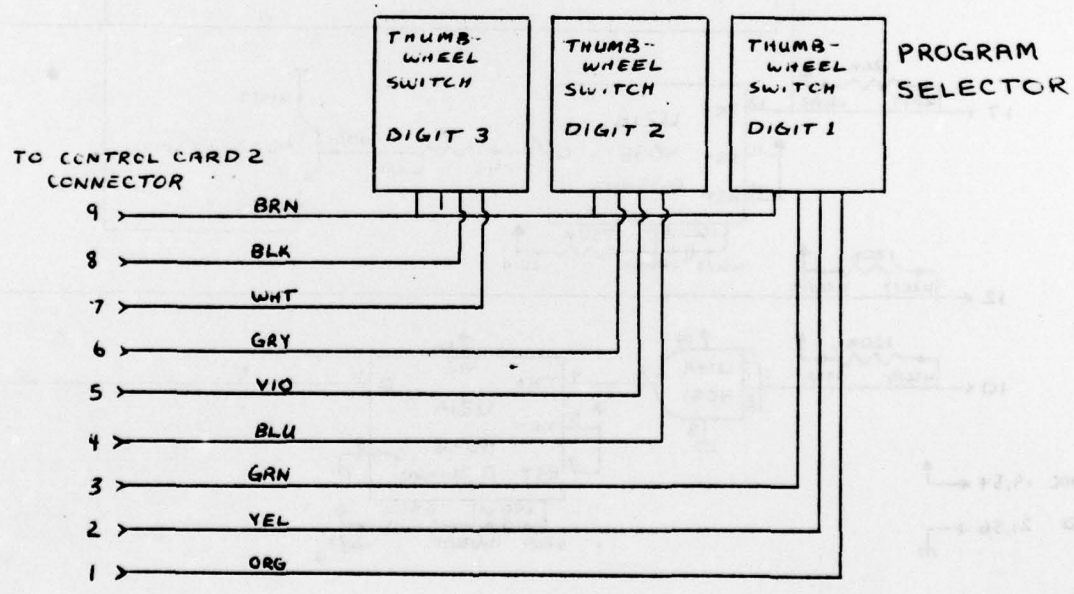
CONTROL CARD 1 SCHEMATIC DIAGRAM



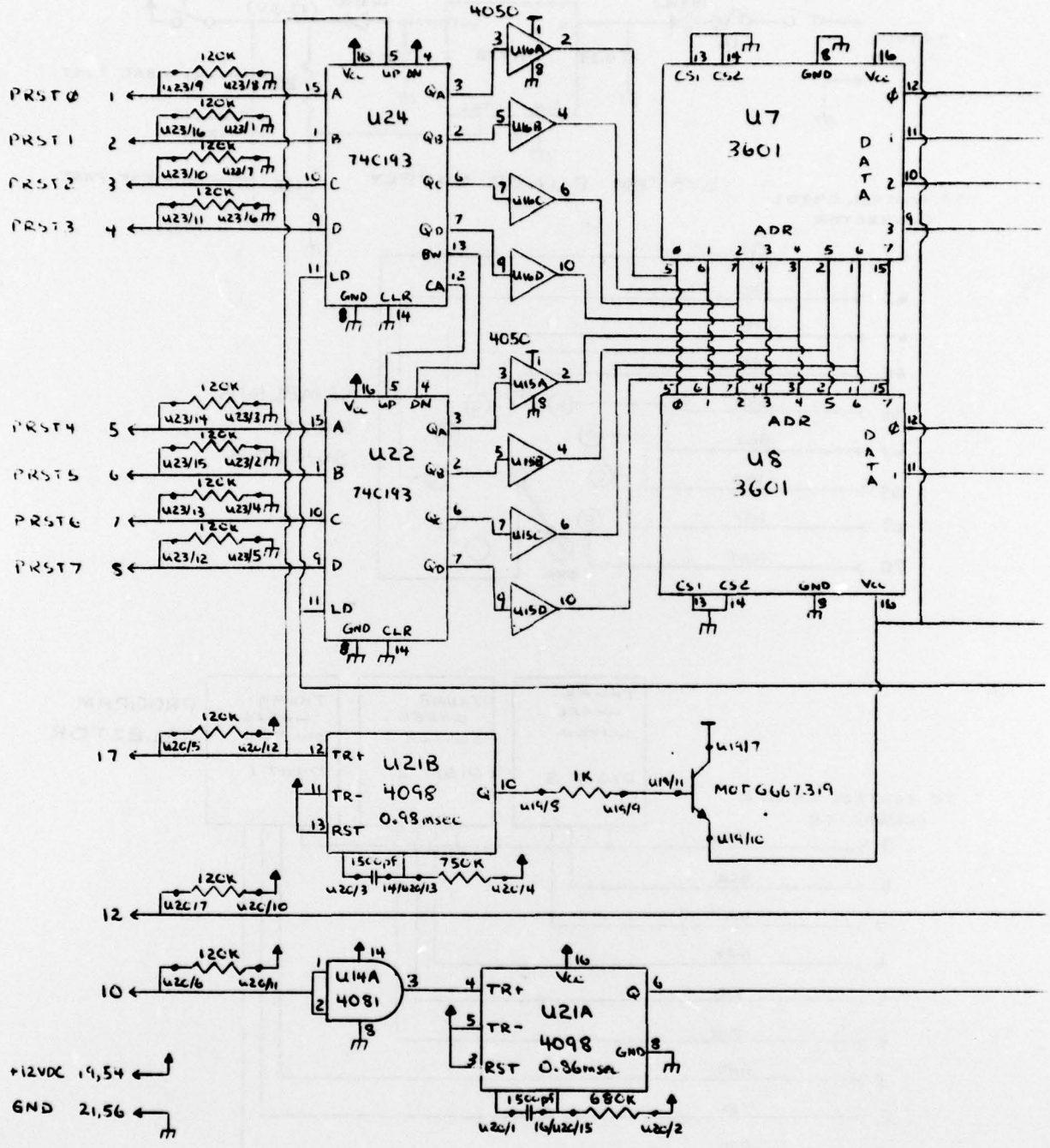
CHASSIS WIRING SCHEMATIC DIAGRAM



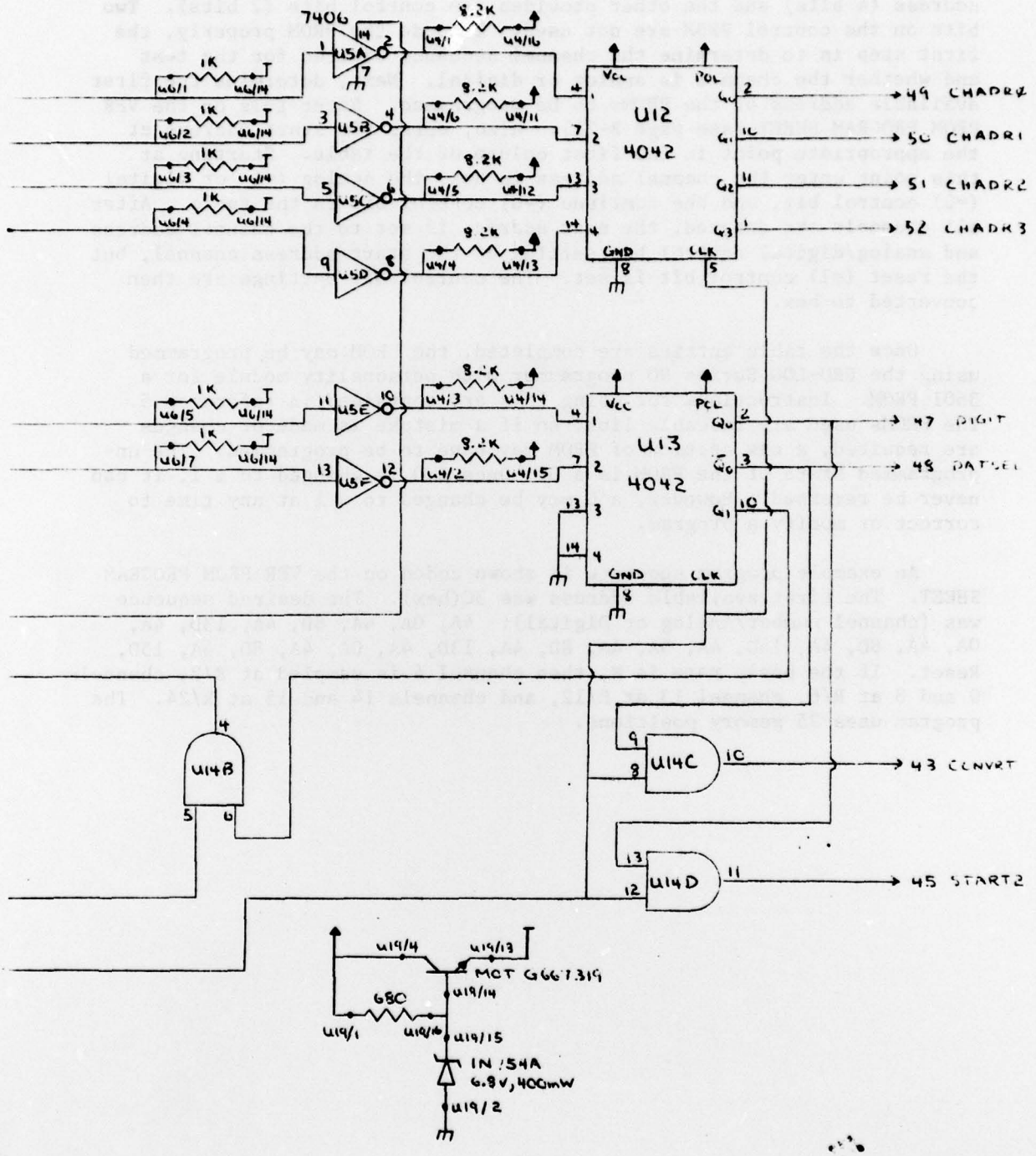




CONTROL CARD 2 SCHEMATIC DAIGRAM



CONTROL CARD 2 SCHEMATIC DIAGRAM



PROM PROGRAMMING INSTRUCTIONS

Two PROMs are used on the control card. One provides the channel address (4 bits) and the other provides the control bits (2 bits). Two bits on the control PROM are not used. To code the PROM properly, the first step is to determine the channel sequence desired for the test and whether the channel is analog or digital. Next, determine the first available address of the PROMs to be programmed. Enter this on the VPR PROM PROGRAM SHEET (see page B-21). Also, enter the start address at the appropriate point in the first column of the table. Starting at this point enter the channel address in hex, the analog (=1) or digital (=0) control bit, and the continue (=0) control bit in the table. After all channels are entered, the next address is set to the channel address and analog/digital control bit setting of the start address channel, but the reset (=1) control bit is set. The control bit settings are then converted to hex.

Once the table entries are completed, the PROM may be programmed using the PRO-LOG Series 90 programmer with personality module for a 3601 PROM. Instructions for doing this are contained in reference 5. The PROMs used are fuseable link, so if a mistake is made or changes are required, a new section of PROM may have to be programmed. The unprogrammed state of the PROM is a 0. Once a 0 is changed to a 1, it can never be reversed. However, a 0 may be changed to a 1 at any time to correct or modify a program.

An example program sequence is shown coded on the VPR PROM PROGRAM SHEET. The first available address was 3C(hex). The desired sequence was (channel number/Analog or Digital): 4A, 0A, 4A, 8D, 4A, 13D, 4A, 0A, 4A, 8D, 4A, 14D, 4A, 0A, 4A, 8D, 4A, 13D, 4A, 0A, 4A, 8D, 4A, 15D, Reset. If the basic rate is R, then channel 4 is sampled at R/2, channels 0 and 8 at R/6, channel 13 at R/12, and channels 14 and 15 at R/24. The program uses 25 memory positions.

VPR PROM PROGRAM SHEET

TEST: M151 6 channel PROM NO: ØØ1

PROM START ADDRESS(HEX): 3C PROM START ADDRESS(OCTAL): Ø74

PROM ADRS HEX	CHNL ADRS/ TYPE	CHNL ADRS HEX	CTRL BITS R=1 A=1	CTRL WORD HEX
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
A				
B				
3C	4A	4	0 1	1
D	0A	0	0 1	1
E	4A	4	0 1	1
F	8D	8	0 0	0
40	4A	4	0 1	1
1	13D	D	0 0	0
2	4A	4	0 1	1
3	0A	0	0 1	1
4	4A	4	0 1	1
5	8D	8	0 0	0
6	4A	4	0 1	1
7	14D	E	0 0	0
8	4A	4	0 1	1
9	0A	0	0 1	1
A	4A	4	0 1	1
B	8D	8	0 0	0
C	4A	4	0 1	1
D	13D	D	0 0	0
E	4A	4	0 1	1
F	0A	0	0 1	1
50	4A	4	0 1	1
1	8D	8	0 0	0
2	4A	4	0 1	1
3	15D	F	0 0	0
4	Reset	4	1 1	3
5				
6				
7				

PROM ADRS HEX	CHNL ADRS/ TYPE	CHNL ADRS HEX	CTRL BITS R=1 A=1	CTRL WORD HEX
8				
9				
A				
B				
C				
D				
E				
F				
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
A				
B				
C				
D				
E				
F				
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
A				
B				
C				
D				
E				
F				

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APPENDIX C - PLAYBACK SYSTEM DATA FORMAT

The output of the LPS-16R is a parallel 16-bit word. The computer compatible tape unit records 8-bit bytes. The tape unit adds an 18-byte header as the first record of the file. A full record contains 2,048 bytes while a partial record will contain at least 18 bytes (padded with zeros to get 18 if necessary). There is no limit on the number of records a file may contain, but there will always be a minimum of two records (a header record plus one data record).

The format of the header byte is 12480000 where the 1, 2, 4, and 8 refer to the binary coded decimal (BCD) value of the header digit and the four least significant digits are always 0. Bytes 1 to 10 contain the ten possible header values and bytes 11 to 18 are all zeros.

The format of the first byte of a data word is $4567890\overset{11}{1}$ where 4, 5, 6, 7, 8, 9, 10, and 11 are the bit numbers of the 12-bit 2's-complement data word. The format of the second byte is ABCD0123 where 0, 1, 2, and 3 are the remaining bit numbers of the 12-bit 2's-complement data word and A, B, C, and D are the four address bits with binary weights of 1, 2, 4, and 8 respectively. The 2's-complement data for an analog channel is decoded as

11 10 9 8 7 6 5 4 3 2 1 0	
1 0 0 0 0 0 0 0 0 0 0 0	+5.0000 V
1 1 0 0 0 0 0 0 0 0 0 0	+2.5000
1 1 1 1 1 1 1 1 1 1 1 1	+0.0024
0 0 0 0 0 0 0 0 0 0 0 0	0.0000
0 0 0 0 0 0 0 0 0 0 0 1	-0.0024
0 0 1 1 1 1 1 1 1 1 1 1	-2.5000
0 1 1 1 1 1 1 1 1 1 1 1	-4.9976

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APPENDIX D - DETAILS OF READOUT UNIT

A block diagram of the readout unit is in figure D-1. The LPS-16R inputs and outputs are TTL compatible so the readout unit was constructed using TTL devices. The four address lines go directly to a binary to binary coded decimal (BCD) converter. The converter drives a latched display which holds the address until the next word is output. The data lines are coded in 2's-complement format. The most significant bit indicates the sign of the data. This bit is used to drive eleven gated inverters which invert the other data bits if the sign is negative and do nothing if the sign is positive. Thus, the 2's-complement data is converted to straight binary plus a sign bit. The binary data then goes to a binary to BCD converter which in turn drives the data display. The WORD SYNC signal from the LPS-16R is used to latch the data and address displays. A push button on the front panel of unit is connected to a monostable multivibrator which generates a short pulse to advance the LPS-16R to the next word on tape when desired.

In order for the LPS-16R to read a single word from tape, a file gap must be recorded after every word. This is accomplished by setting the proper jumper on the formatter card of the LPS-16. With a file gap written after every word the maximum recording rate is two channels per second and a tape will hold only 60,000 words. If the file gap is not set for a gap after every word, the readout will display only the last word in the file.

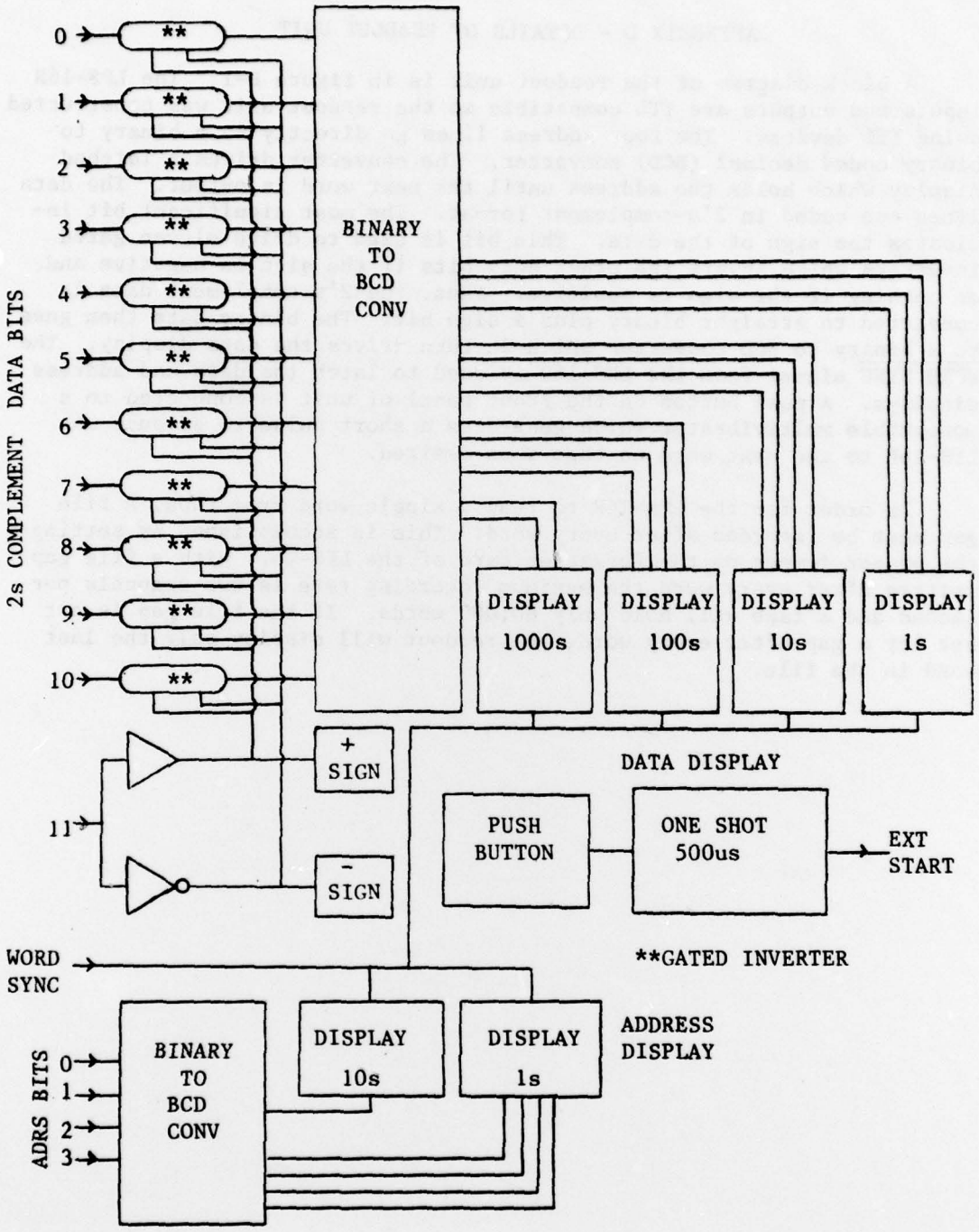

Figure D-1. Block diagram of readout unit.

APPENDIX E - DETAILS OF CALCULATOR INTERFACE

A block diagram of the calculator interface is in figure E-1. A Hewlett-Packard 98032A 16-bit parallel interface card is used with the 9825 calculator. All inputs and outputs of the 98032A are designed to work with open collector TTL ICs. The inputs and outputs of the LPS-16R are not open collector compatible. The 16 data lines from the LPS-16R are buffered by open collector drivers before going to the 98032A. Reading of data is initiated by setting CTLO of the 98032A high. This action resets the pulse counter and turns on the EXT START line of the LPS-16R which begins the reading process. As each word is output, the WORD SYNC increments the counter and is buffered by an open collector driver setting PFLG which tells the interface to latch the data. After 2,040 words are output by the LPS-16R, the counter output goes low, turning off the EXT START which stops the LPS-16R. At the same time, the EXT START signal is gated to EIR which tells the calculator the data transfer is complete. The calculator may then process the 2,040 words. If the end of data is reached before 2,040 are counted, a missing pulse detector combined with a 3-second delay circuit triggered by EOF detects this and is gated to EIR to tell the calculator the data transfer is complete.

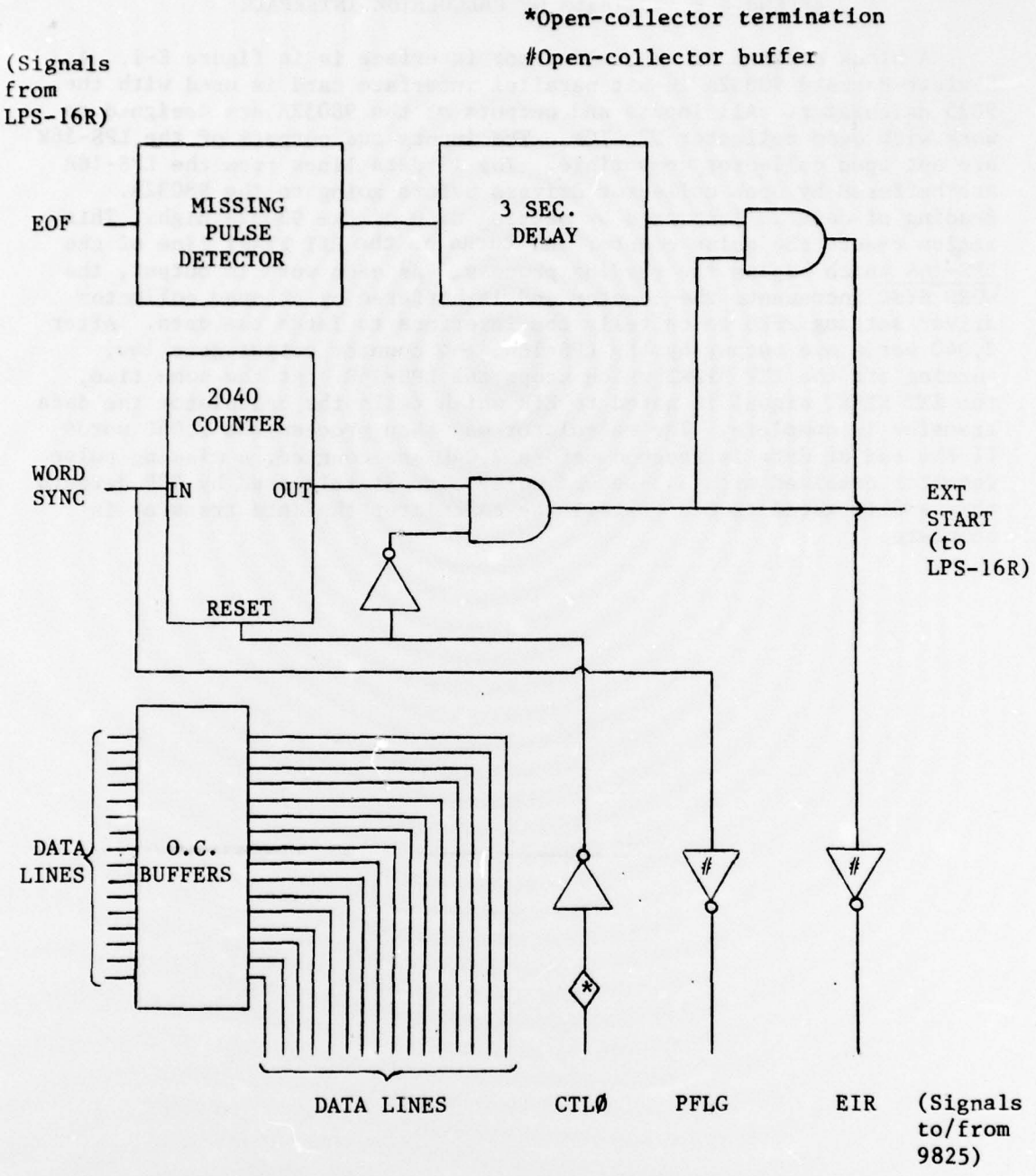

Figure E-1. Block diagram of calculator interface.

APPENDIX F - ABBREVIATIONS

A/D = analog to digital
BCD = binary coded decimal
CMOS = complimentary metal oxide semiconductor
MSMV = monostable multivibrator
PCM = pulse code modulation
PROM = programmable read-only memory
TTL = transistor-transistor logic
VMS = vehicle monitoring system
VPR = vehicle performance recorder

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